Table of Contents

MTP	MTE	bottom side, 22mil
TP	EE/SW debug	top side, 22mil
XDP_TP	Intel requested	don't care, 22mil
GTP	Unused IO and GPIO/ Possible for Future Removal	don't care, 22mil
PTP	Current Sensing	top side (as close to resistor as possible), 22mil
MTP_BF	MTE big pads for FW, OS load, and RF.	bottom side, 31mil
MTTP_BF	MTE big pads for RF	top side, 31mil (if RF connector at the bottom side of the board)

CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

Title: 01. Table of Contents

Microsoft Confidential | Engineer: Surface

Size	Project Name	Rev
A3	A	1.0.0.1

Date: Thursday, April 26, 2018 | Sheet 1 of 79

Schematics Change History

Schematics Change is maintained in spreadsheet, and would not fit on this page.

CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors

Property: BUILD-OPT

DNP = Not Installed Part.

S = Short after design fixed

Title: 02. CHANGE HISTORY			
Microsoft Confidential	Engineer:	Surface	
Size: A3	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 2 of 79		

Architectural Diagram I-Core

Rev 2.5

Front IR (OV7251)

Illuminator

Debug UART, external connector

Power Monitor Components (DEBUG)

MIPI CSIx1 (1Gbps)

I2C

MIPI CSIx1

Front RGB (720p – OV9734)

Analog audio combo jack (3.5mm)

HD Audio

I2C

Audio Codec

R

L

AMP ALC1304

Right

Left

2 Mic

3.3V@0.8A OUT

Memory/ Storage

SSD2 BGA chip 128GB, 256GB 512GB, 1TB

SSD BGA chip 128GB, 256GB 512GB, 1TB

LPDDR3 x32 16,8,4 GB (4x)

2/4 x PCIe

2/4 x PCIe

128-bit (32b x 4) – 2 Chl -64 bit each

ALS

I2C

I2C1 UART2 CSI2x2 CSI2x2 I2C2

HDA I2C4

I2C3

PCIe 11/12

PCIe 7/8

DDR0x64, DD1x64

DMIC

DDI1

DDI1_AUX

DDPB_CTRL

DDI2_AUX

DDPC_CTRL

USB3p2

USB2p2

DDI2

16MB SPI ROM

Quad SPI

SPI0 GPIOs

Backlight Controller

I2C5

LCD 13.5"

TCON

NTRIG G5

eDP

eDP 1.4a

SPI

SPI1

I2C

I2C0

INT

SKL-U 15W 2+2/2+3E

DDI2_AUX

DDPC_CTRL

USB3p1

USB2p1

PCIe9

USB2p5 LPC

UART

UART1

DPG

PDX

TrackPad

KeyBoard

UART

INT

SC Freescale K22

UART

SL UART

MUX

PWM/Tach

Fan/Fan Connection

Temp

I2C

I2C

SC Debug

Hall Effect

XDP

Debug XDP

LPC

1XPCIe

USB2

Wifi abgn+ac Marvell 88W8897 BT

Antennas

Power path updates Separate Block Diagram

POR CHANGES

TPM Infineon Nuvaton NationZ

IMVP8 PMIC ISL95857 W/2+3E support

Power/PMIC BD9992GW (sep Block Dia)

7.4V

Battery 45WH w/Fuel G

7.4V

Battery Charger ISL9237

SC,K22

Greenpak

Surflink

SD FLUSH

POR CHANGES

2xTPS62134 VCCEDRAM/VCCEOPIO

MUX

AUX/DDPC

CMC + ESD

mDP

POWER IN/OUT

MUX

AUX/DDPC

Debug Signals

Debug MUX

CMC + ESD

CMC + ESD

5V@1.78A OUT

CMC + ESD

USB2

POR CHANGES

LEGEND

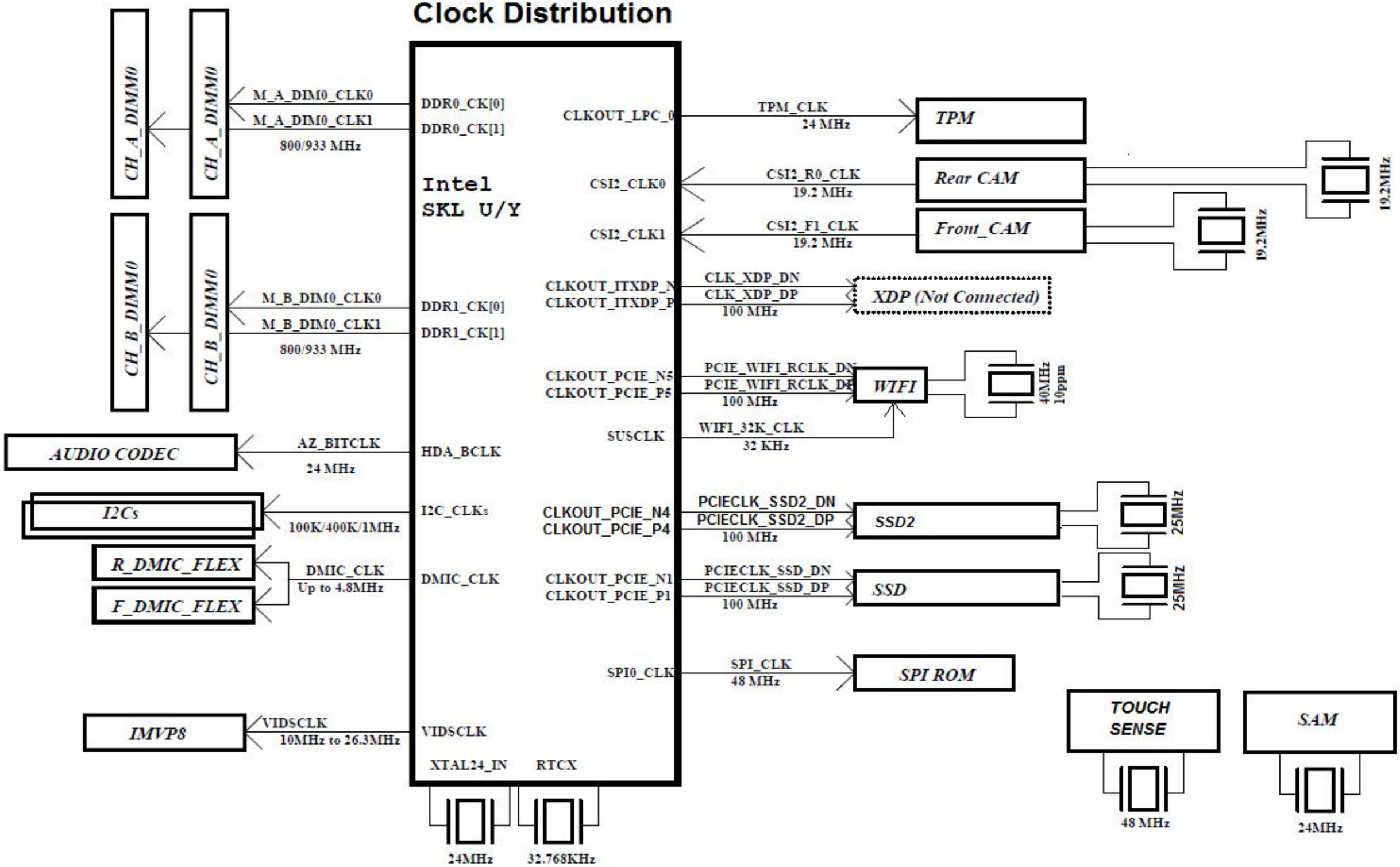
Mostly same as P

Changed Feature/Implementation

New Feature/Implementation

Title:	03. BLOCK DIAGRAM		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 3 of 79		

Clock Distribution



Title: 04. CLOCK DISTRIBUTION			
Microsoft Confidential	Engineer: Surface		
Size: A3	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 4 of 79		

System Power State Diagram

3P3VA ON
3P3V_SAMON
S0 RAILS ON

3P3VA ON
3P3V_SAMON
S0 RAILS OFF

3P3VA ON
3P3V_SAMOFF
S0 RAILS OFF

3P3VA OFF
3P3V_SAMOFF
ALL S0 RAILS OFF

S5
S5 PWR:ON / S0 OFF
SAM: Active
GP/RTC: ON

S0
S5/S0 Pwr: ON
SAM: Active
GP/RTC: ON

Pre-S5
S5/S0 PWR:OFF
SAM: Active
GP/RTC: ON

Connected Standby
S5/S0 Pwr: Low Power
SAM: Low Power
GP/RTC: ON

DeepSlp
S5/S0 PWR: OFF
SAM: OFF
PMIC/CHGR: OFF
GP/RTC: ON

Any State
(except EMER Shutdown)

EMER Shutdown
S5/S0 PWR: OFF
SAM: OFF
PMIC/CHGR OFF
GP/RTC: OFF
BATTERY:OFF

G3
S5/S0 PWR: OFF
SAM: OFF
PMIC/CHGR OFF
GP/RTC: OFF

Hard Reset
S5/S0 PWR: OFF
SAM: Pwr Cycle
PMIC/CHGR:Pwr Cycle
GP/RTC: ON

HW Debug
S5/S0 PWR: OFF
SAM: Pwr Cycle
PMIC/CHGR:Pwr Cycle
GP/RTC: ON

Battery/System Critical Temp (SAM)

OS Shut Dowm

SB_PWRBTN Asserted (debounced PWR_SW_N)

PMIC_EN de-asserted

PMIC_EN AND (PWR_SW_N OR PWR_BTN_STATE) asserted)

SB_PWRBTN asserted OR Keyboard Lid Closed OR Sleep Selected OR OS Timeout

SB_PWRBTN asserted OR OS Wake Event

Battery/System Critical Temp (SAM)

SAM_GP_DEEPSLP Asserted (no PSU & 30s timeout)

PWR_SW_N asserted >30msec OR SL_PG asserted

Surflink PWR applied

Surflink PWR applied

VDD_BAT PWR applied

GP_DBACC asserted AND Hard Reset Done

Hard Reset Done (PWR_BTN_STATE asserted)

System Temp Critical (HW GP_TSYS>Tcrit OR Bat temp>60C)

SAM_RST asserted OR PWR_SW_N >15s

PWR_SW_N >30sec

NOTE: HW Debug state only available during development

Title:	05. SIGNAL & RESET MAP		
Microsoft Confidential	Engineer:	Surface	
Size: C	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 5 of 79		

J47001
SurfLink Connector
PWR_SL1

PWR_SL1

Q63008 / Q63009
Back to Back FETS

PWR_SL1_R

R63001
20mΩ

U63001
ISL9237
Buck/Boost Charger

VSYS_R

R63042
10mΩ

R63009
10mΩ

VDD_BAT

J70001 /70002 / 70003
Battery Connector

2S
Battery
7.6V typ

VDD_BAT

PWR_SL1_F

3P3VA
Imax = .5A

U56002
TPS 62177
3P3VA
Always On

R56007
100mΩ

U56005
NX3P1108
3P3VA_SW_EN

R56033
100mΩ

3P3VA_SW
Imax = .3A

R36016
100mΩ

3P3VA_TEMP

R36023
100mΩ

3P3V_PMI_DBG

R28001
100mΩ

3P3VA_SAM

R31023
0mΩ

3P3V_DEBUG

VCC_RTC
Imax=100 uA

IMVP 8

VCORE

VCCGT/GTx

VCCSA

R67007
20mΩ

R68001
20mΩ

R67028
50mΩ

VCORE

VCCGT

VCCSA

SKL
VCORE
Imax = 28A
VCCGT/VCCSC
Imax = 10A
VCCSA
Imax = 7A

Platform PMIC
U58001

V3P3_DSW
V6

R58034
10mΩ

V3P3_DSW

R58039
20mΩ

R26004
10mΩ

3VSUS_ORG

R88001
100mΩ

3P3V_TPM

U65003
TPS22920
3P3V_SSD_EN

R6501010mΩ

3P3V_SSD

R43017
25mΩ

U43005
TPS 62085
1P8V_SSD

1P8V_SSD

R43016
25mΩ

U43006
TPS 62085
1P2V_SSD

1P2V_SSD

U65001
TPS22920
EDP_VDD_EN

R65002
50mΩ

3P3V_PANEL

U53005
NCP380
nDP_PWR_EN

R53037
0Ω

ML_V3P3_PWR

J53001
mDP
Connector

R54035
100mΩ

3P3V_CAM

V5A
V5

R58019
5mΩ

V5A

R58024
10mΩ

R45003
5mΩ

U45004
AP2553
SKL_SLP_S4_N

5V_USBPWR_A

J45001
USB 3.0 A
Connector

R48022
100mΩ

U48002
SLG59M1448V
PCH_TPANEL_PWR_EN

5V0_OFFBOARD
(keyboard)

R64029
10mΩ

5V_SWPWR

R64006
50mΩ

U64002
SLG59M1448 V
PCH_TPANEL_PWR_EN

5V_TS

R64016
20mΩ

U64004
SLG59M1448V
PCH_AUD_5V_EN

5V_AUDIO

R64020
20mΩ

U64006
SLG59M1448V
SAM_FAN_PWR_EN

5V_FAN (i-core only)

Vsys

V1P8A
V8

R58012
20mΩ

V1P8A

R58016
20mΩ

R28003
10mΩ

1P8VSUS_ORG

U62001
SLG59M1448 V
PCH_AUD_1V8_EN

R62002
20mΩ

1P8V_AUDIO

R40005
20mΩ

1P8V_AUDIO_DVDD

U62003
NX3P1108
PCH_TPANEL_PWR_EN

R62007
20mΩ

1P8V_TS

V3P3A_PCH
V7

R58002
10mΩ

V3P3A_PCH

R58008
50mΩ

U65004
TPS 22920
WWAN_PWREN

R65012
40mΩ

3P3V_WWAN

V0P85A
V12

R59023
25mΩ

V0P85A

R59027
10mΩ

V0P85A

V1P00A
V11

R59003
25mΩ

V1P00A

R59007
10mΩ

V1P00A

R61007
20mΩ

1V_MODPHY

U61002
SLG5NT1477
VCCSTG_EN

R61003
10mΩ

VCCSTG

U61003
SLG5NT1477
SKL_SLP_S4_N +
XDP_PRESENT_LOGIC

R61006
10mΩ

VCCST_CPU

R18001
0mΩ

V1P00A_XDP

V1P8U_2P5U
V9

R58023
10mΩ

V1P8U_2P5U

R58026
50mΩ

V1P8U_2P5U

V1P2U
V10

R58032
25mΩ

V1P2U

R58037
5mΩ

R59032
10mΩ

U61001
SLG5NT1477
SOIX_EN

R61005
10mΩ

VCCPLL_OC

V0P6DX_LPDDR3
V13

R59035
20mΩ

V0P6DX_LPDDR3

VCCIO
V4

R58004
25mΩ

VCCIO

R58030
10mΩ

VCCIO

U72001
RT8555
L_BKLTEN

R72001
20mΩ

VCC_EDP_BKLT_OUT

DeepSleep Rail

S4/S5 Rail

S0 Rail

Power Monitor Input

R99999
20mΩ

Load switch
Control Signal

DC-DC
Regulator

External
Regulator/Load
Switch

Linear
Regulator

DVT/U70850x16x512xCRetail

Title: 06. POWER DISTRIBUTION

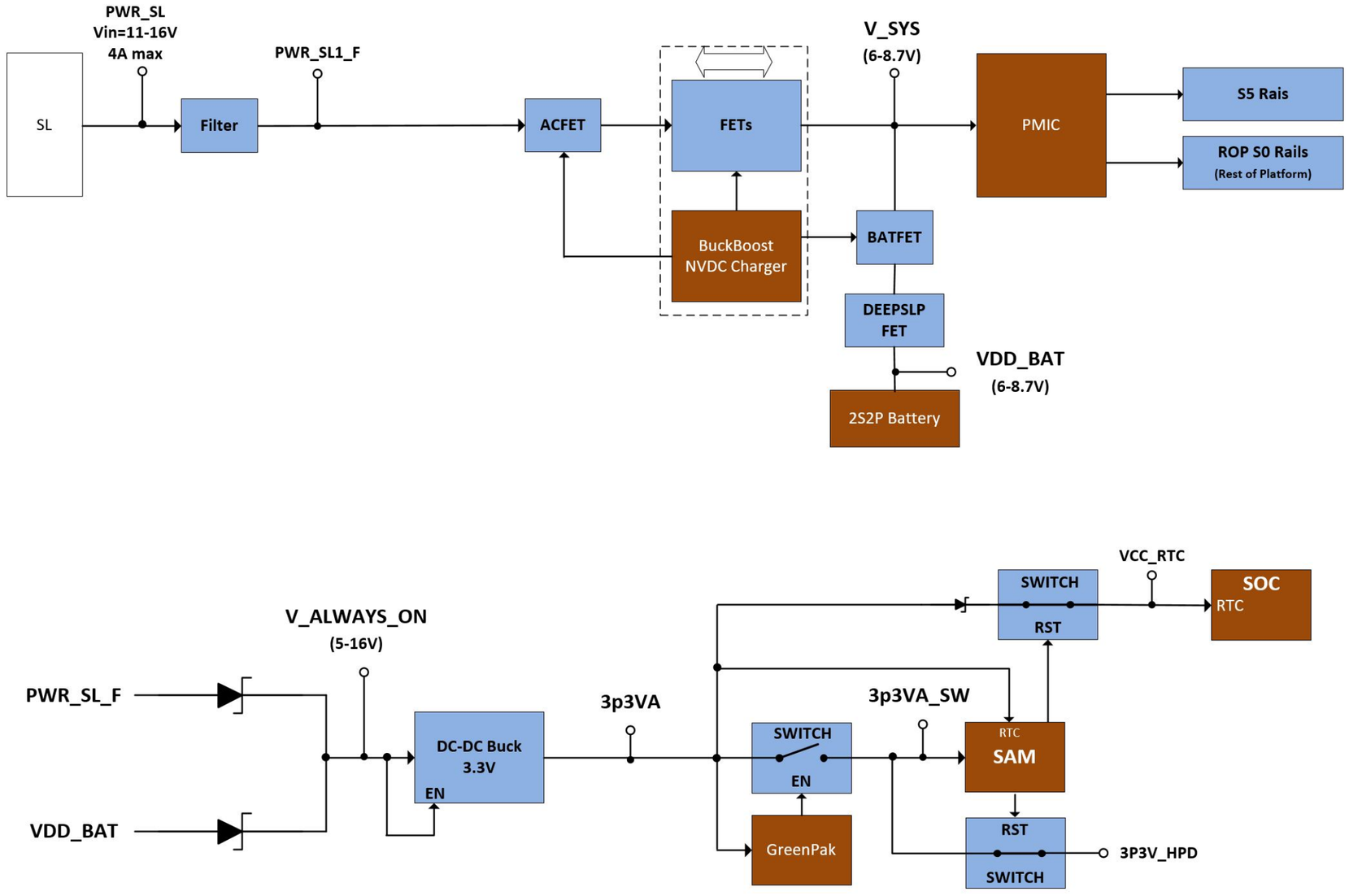
Microsoft Confidential

Surface

Size	Project Name	Engineer	Rev
Custom	A		1.0.0.1

Date: Thursday, April 26, 2018 Sheet 6 of 79

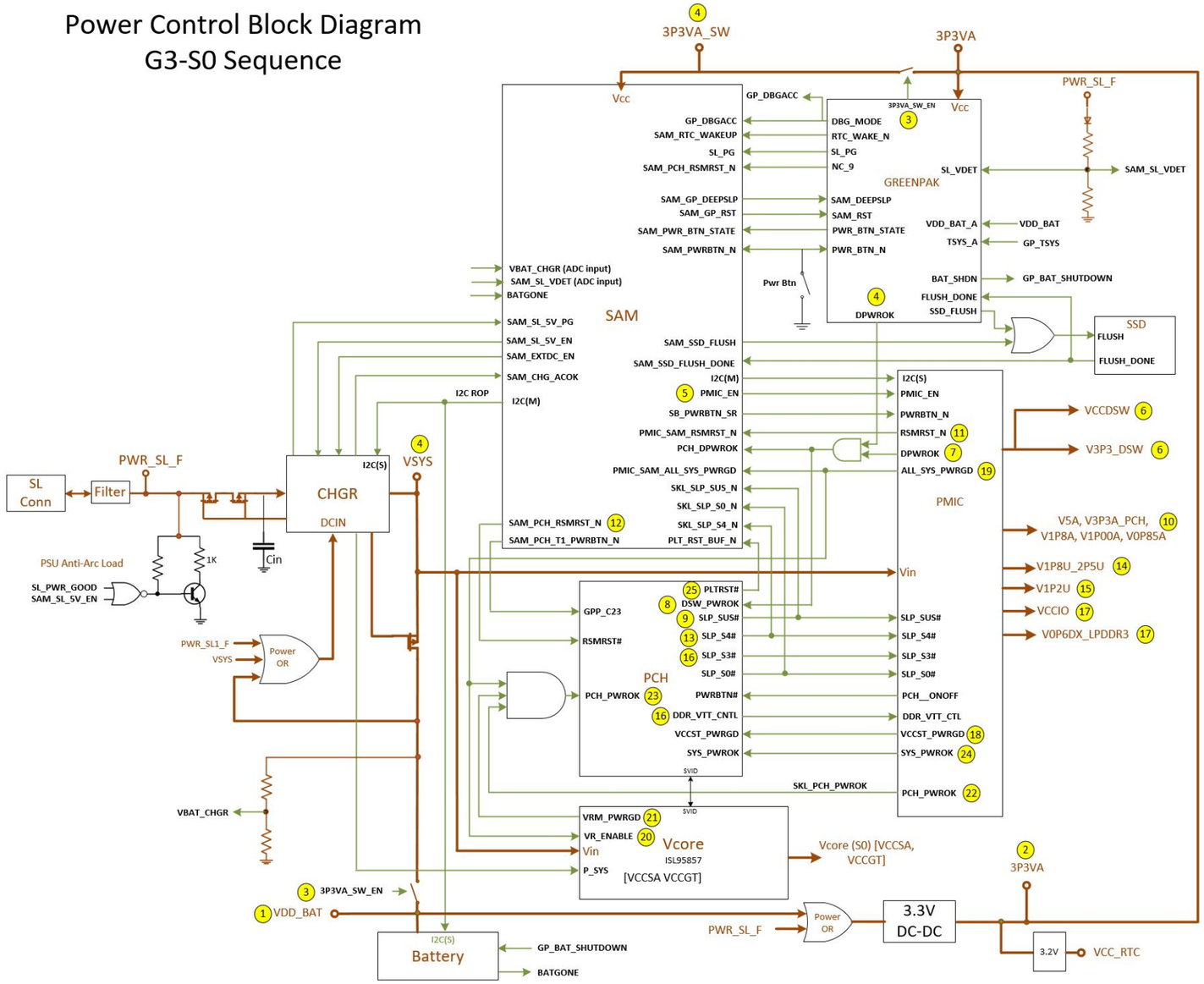
Lynx SL INPUT POWER DIAGRAM



DVI7U7680s16s512x2Retail

Title:	07. POWER SEQUENCE 1		
Microsoft Confidential	Engineer: Surface		
Size: D	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 7 of 79		

Power Control Block Diagram
G3-S0 Sequence



DVI7U7660s16s512x2Retail

Microsoft Confidential		Engineer: Surface	
Size: D	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018		Sheet 8 of 79	

Title: 08. POWER SEQUENCE

I2C Map

7-bit slave addresses
September 28, 2016

DEBUG: Power Monitors

U36002 PMI1 MAX34407 0x12 S
U36004 PMI3 MAX34407 0x18 S
U36006 PMI5 MAX34407 0x1C S
U36008 PMI6 INA231 0x41 S
U36001 PMI0 MAX34407 0x1E S
U36003 PMI2 MAX34407 0x10 S
U36005 PMI4 MAX34407 0x1A S
U36007 PMIBATT INA231 0x40 S

3P3V_PMI_DBG — 2.2k? — To EE Power Debug Connector
PMI_I2C_Sxx
Option to connect to I2C_ROP_Sxx

Debug Connector
EE Power Debug Connector
Debug Muxes
Removed in Retail
DEBUG_OSG in Retail
DNP in Non-Retail/Retail

Cameras

EEPROM GT24C08S 0x50, 0x51, 0x52, 0x53 S
Front RGB OV9734 0x36 S
IR Cam OV07251 0x60 S

1P8VSUS_ORG — 2k? — I2C_Sxx_CAM — To EE Power Debug Connector

Light Sensor and BKLT Controller

ALS ISL29033 0x44 S — I2C_Sxx_ALS
Backlight Drvr RT8555 0x31 S — I2C_Sxx_BKLT
1P8VSUS_ORG — 2k?
Display_VDD18 — 3P3V_PANEL — 4.7k?
To Debug Connector

Display

TCON MLTS152000 0x28 S — I2C_DISPLAY_Sxx (DNP)
To Debug Connector

SOC/PCH U10001 0x4D

M I2C2
M I2C1
M I2C3
I2C5 M — I2C_Sxx_ALS (DNP) — 1P8VSUS_ORG — 2k? — Option to Connect to ALS Sensor at J54001
I2C0 M — I2C_Sxx_TP
M I2C4

Wifi/BT

Wifi 88W8897 U50001 M
1P8V_WIFI_INT_OUT — 10k? — SER_Sxx
EEPROM AT24C16D S 0x50 -0x57

Trackpad

5VA -> P3V3_TP — TP_PWR_EN — 2.2k?
Trackpad IC S9101B S 0x20
To Debug Muxes
To Debug Connector

Power Management

PMIC BD99992GW 0x30 S — 3P3VA_SW — 2k? — I2C_Sxx_MCU
Charger BQ24770 0x09 S — CHG_Sxx — 3P3VA_SW — 2.2k?
Fuel Gauge BQ40x50 0x0B S — BATT_I2C_xxx
To Debug Muxes
To EE Power Debug Connector

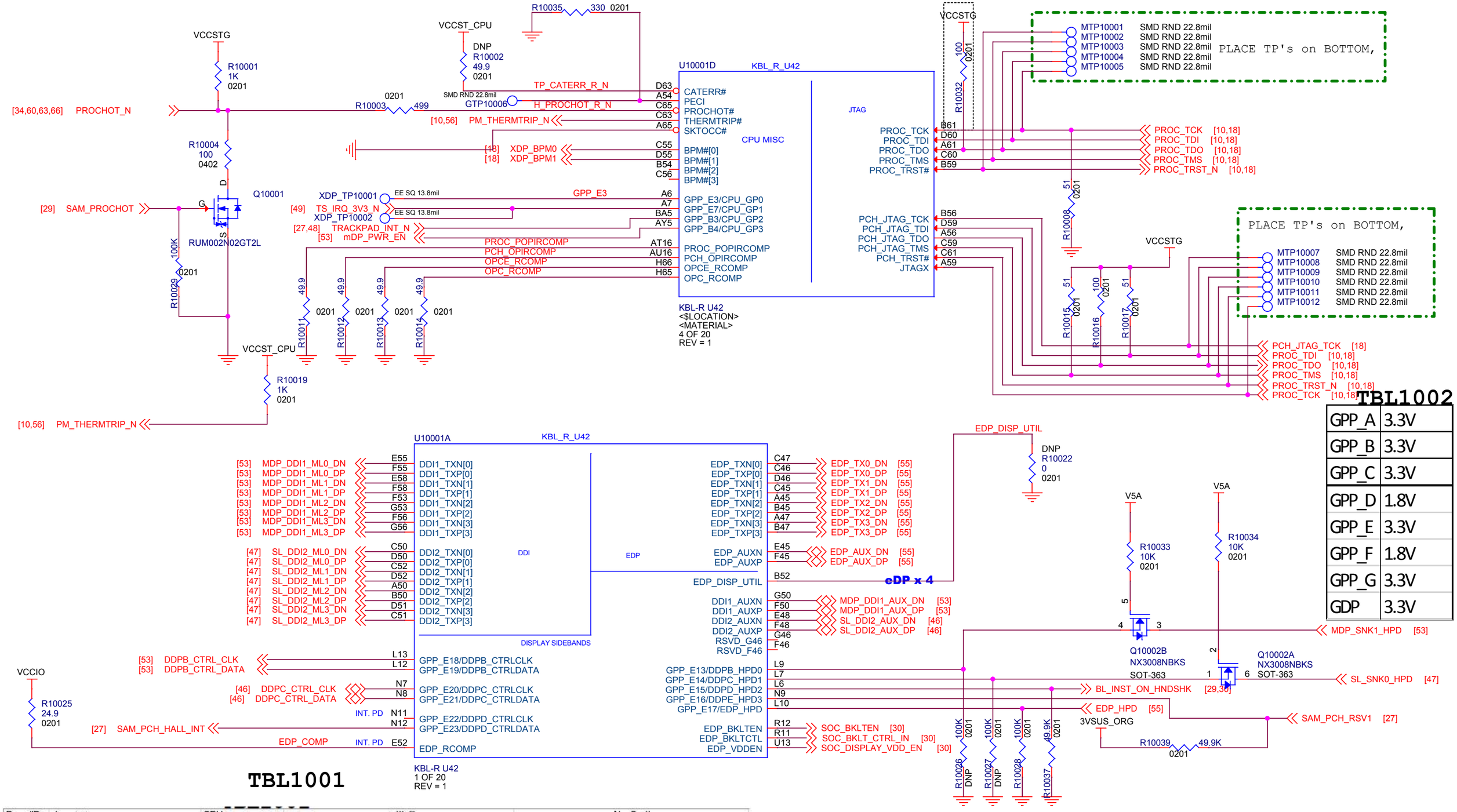
M I2C2
SAM K22P121M120SF5 U27001 0x28
M I2C1 — I2C_ROP_Sxx
I2C0 M — I2C_Sxx_MCU
Option to Connect I2Cs

Temp Sensors

I2C_Sxx_MCU — To EE Power Debug Connector
Critical Temp SN1511004 0x48 S
Temp Sensor STTS751 0x3B S
IR Temp TMP007 0x40 S
Temp Sensor STTS751 0x3A S
Temp Sensor STTS751 0x4A S

DVi7U7660s16s512x2Retail

Title:	09. I2C MAP		
Microsoft Confidential	Engineer:	Surface	
Size: A3	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 9 of 79		



TBL1002

GPP_A	3.3V
GPP_B	3.3V
GPP_C	3.3V
GPP_D	1.8V
GPP_E	3.3V
GPP_F	1.8V
GPP_G	3.3V
GDP	3.3V

TBL1001

BoardID	description	CPU	stuff(all)	No-Stuff
000	reserved		R23040, R23042, R23044	R23041, R23043, R23045, R28091, R28092, R28093
001	reserved		R23041, R23042, R23044, R28091	R23040, R23043, R23045, R28093, R28092
010	KBL U42 i5-8250U	M1086844-00	R23040, R23043, R23044, R28092	R23041, R23042, R23045, R28093, R28091
011	reserved		R23041, R23043, R23044, R28091, R28092	R23040, R23042, R23045, R28093
100	KBL U42 i5-8350U	M1029639-001	R23040, R23042, R23045, R28093	R23041, R23043, R23044, R28091, R28092
101	reserved		R23041, R23042, R23045, R28093, R28091	R23040, R23043, R23044, R28092
110	KBL U42 i7-8650U	M1020597-001	R23040, R23043, R23045, R28093, R28092	R23041, R23042, R23044, R28091
111	reserved		R23041, R23043, R23045, R28091, R28092, R28093	R23040, R23042, R23044

U SPECIFIC

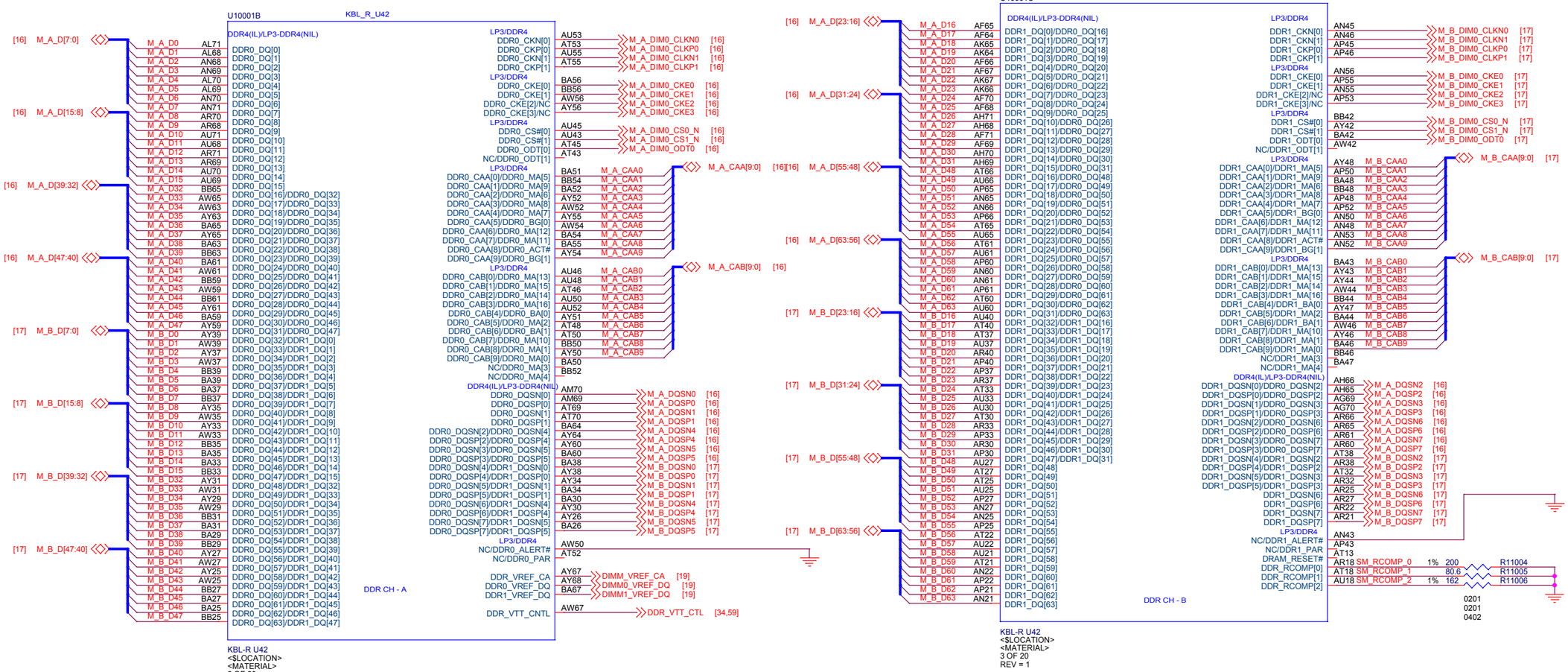
Title: 10. CPU(1)_MISC,JTAG,DDI.EDP

Microsoft Confidential

Engineer: Surface

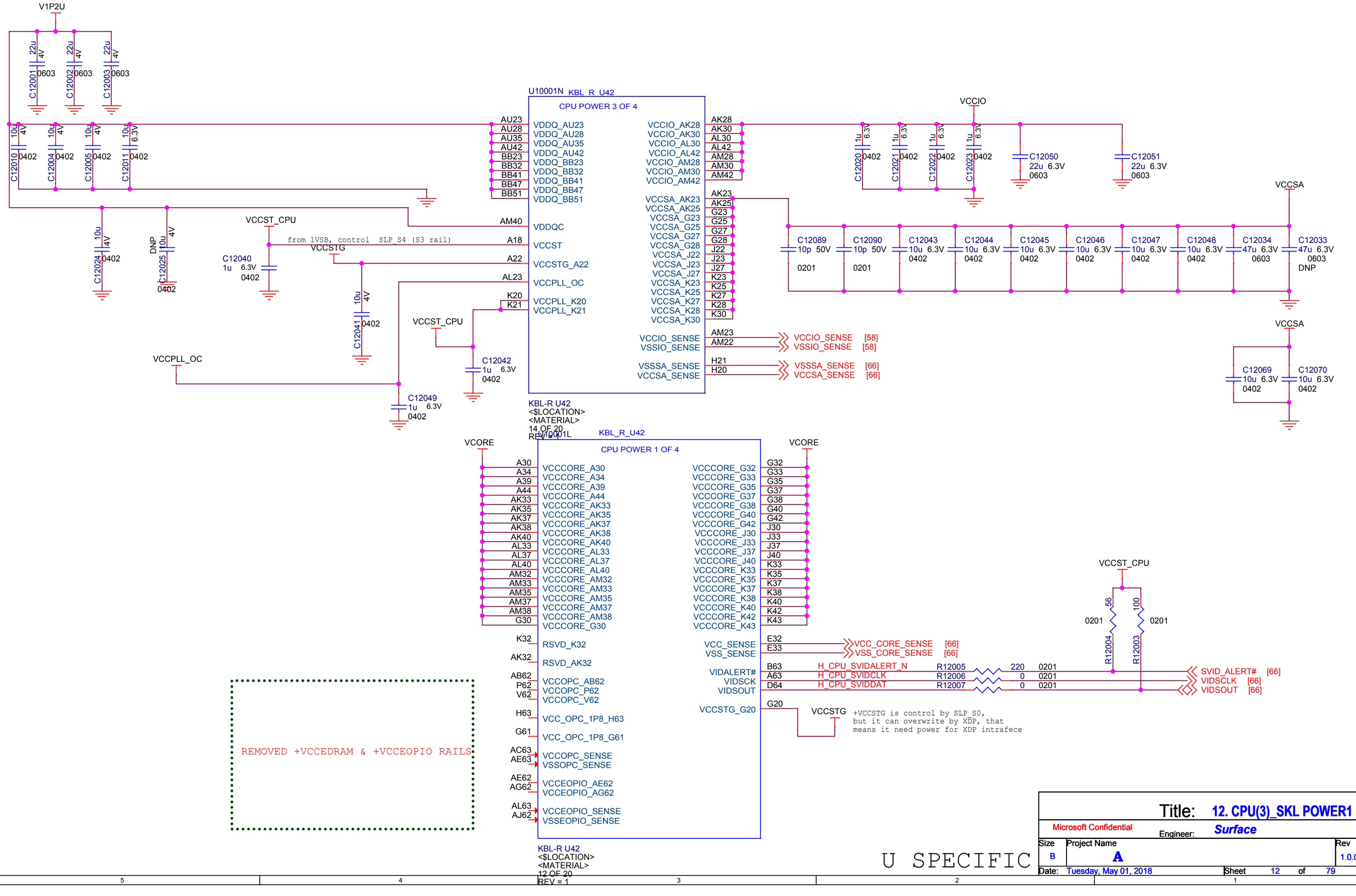
Size	Project Name	Rev
B	A	1.0.0.1

Date: Friday, April 27, 2018 Sheet 10 of 79



U SPECIFIC

Title: 11. CPU(2)_LPDDR3			
Microsoft Confidential	Engineer: Surface		
Size: C	Project Name: A		Rev: 1.0.0.1
Date: Friday, April 27, 2018	Sheet 11 of 79		



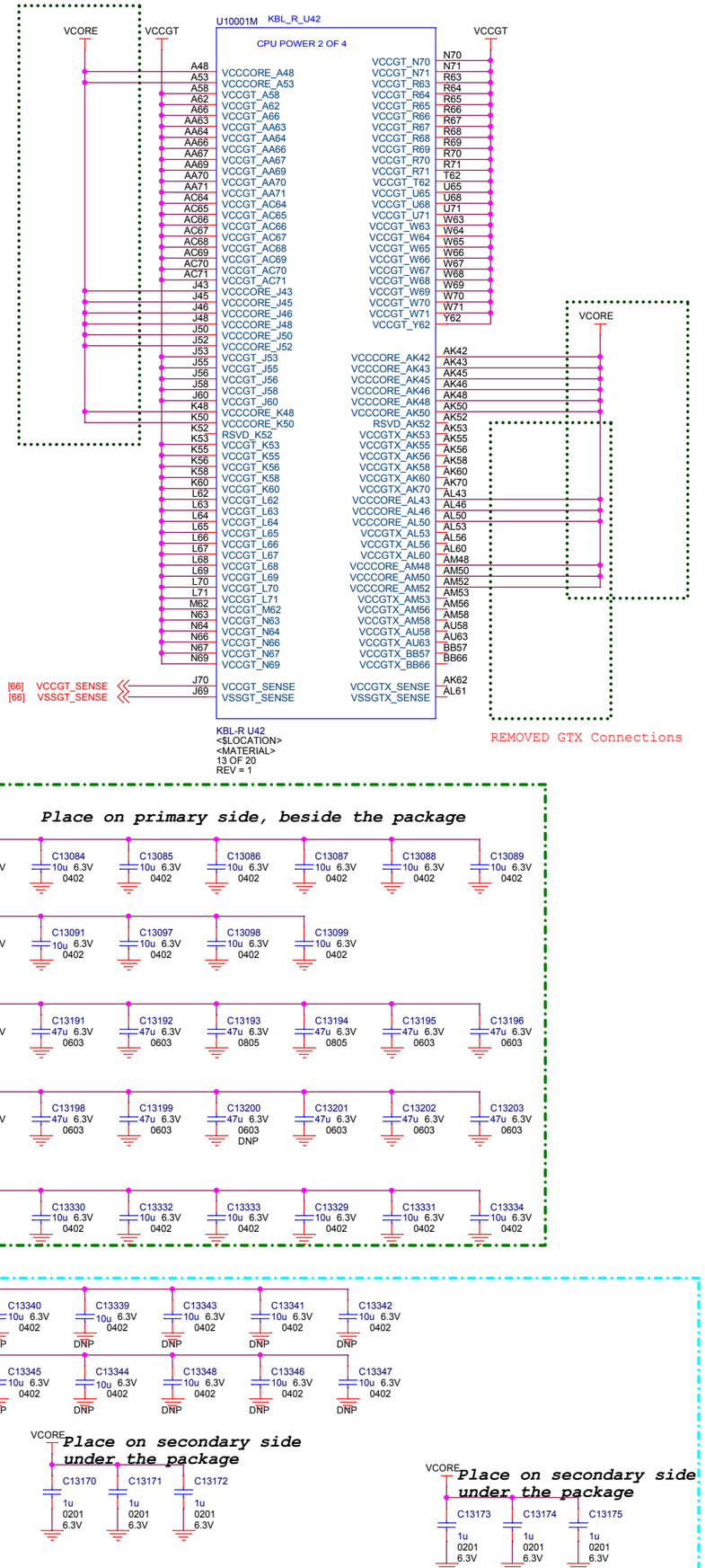
Title: 12. CPU(3)_SKL POWER1

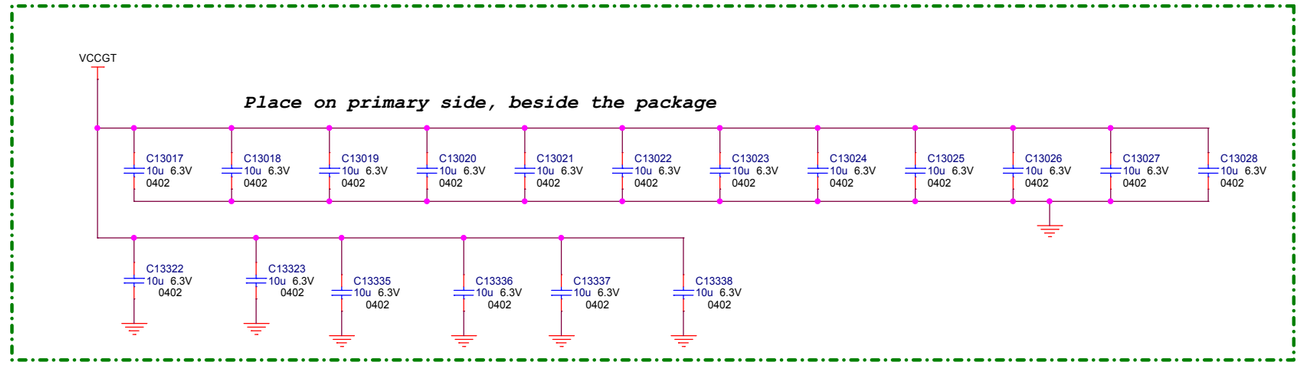
Microsoft Confidential

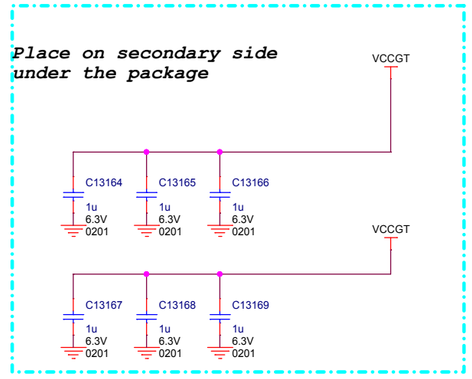
Engineer: Surface

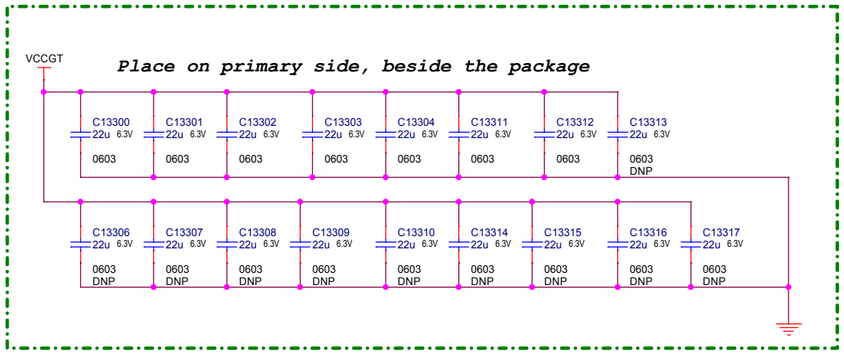
Size	Project Name	Rev
B	A	1.0.0.1

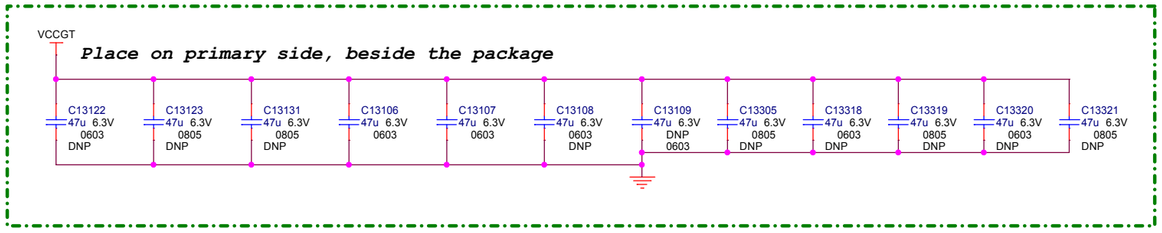
Date: Tuesday, May 01, 2018 Sheet 12 of 79











U SPECIFIC

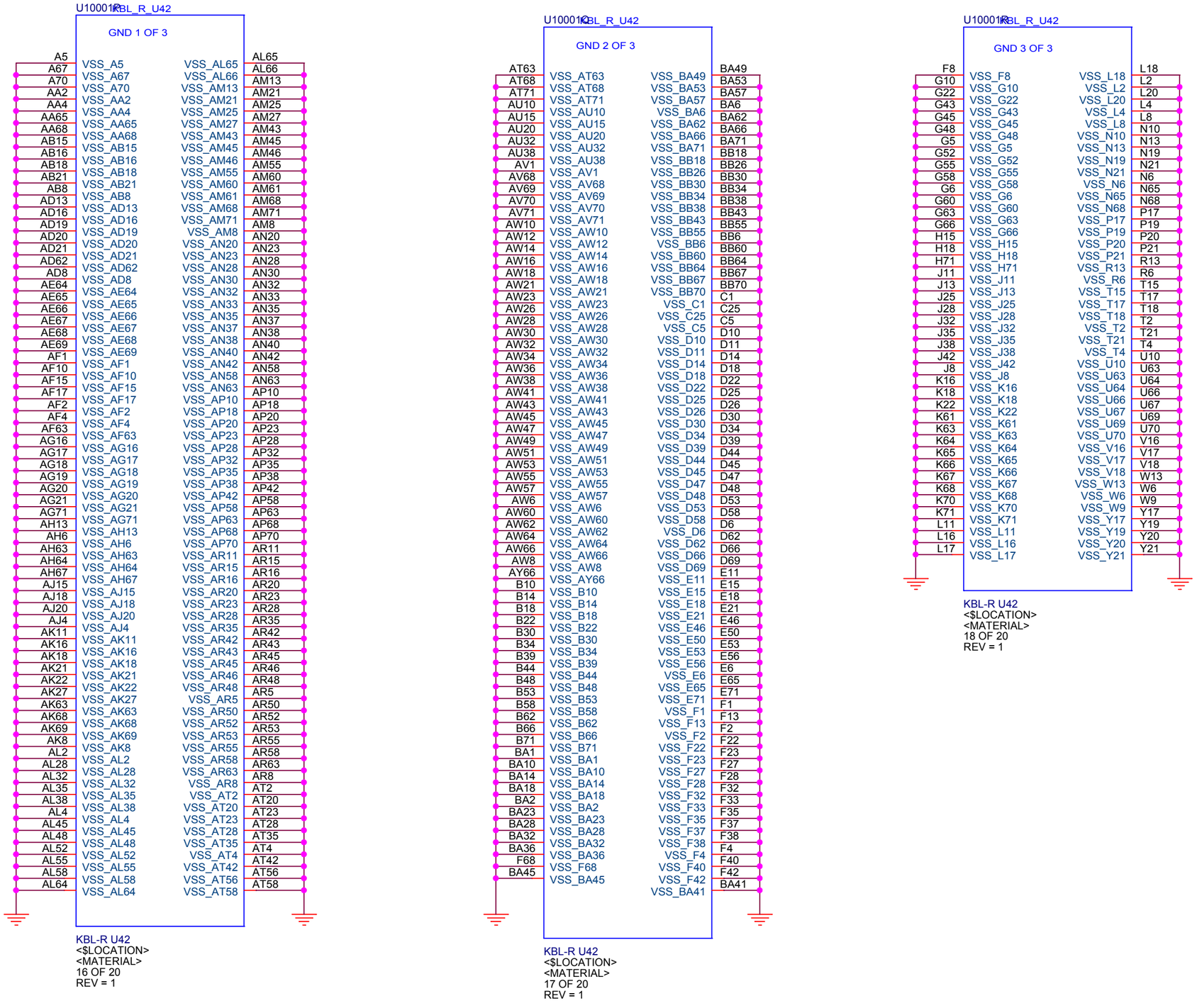
Title: 13. CPU(4)_SKL_POWER2

Microsoft Confidential

Engineer: Surface

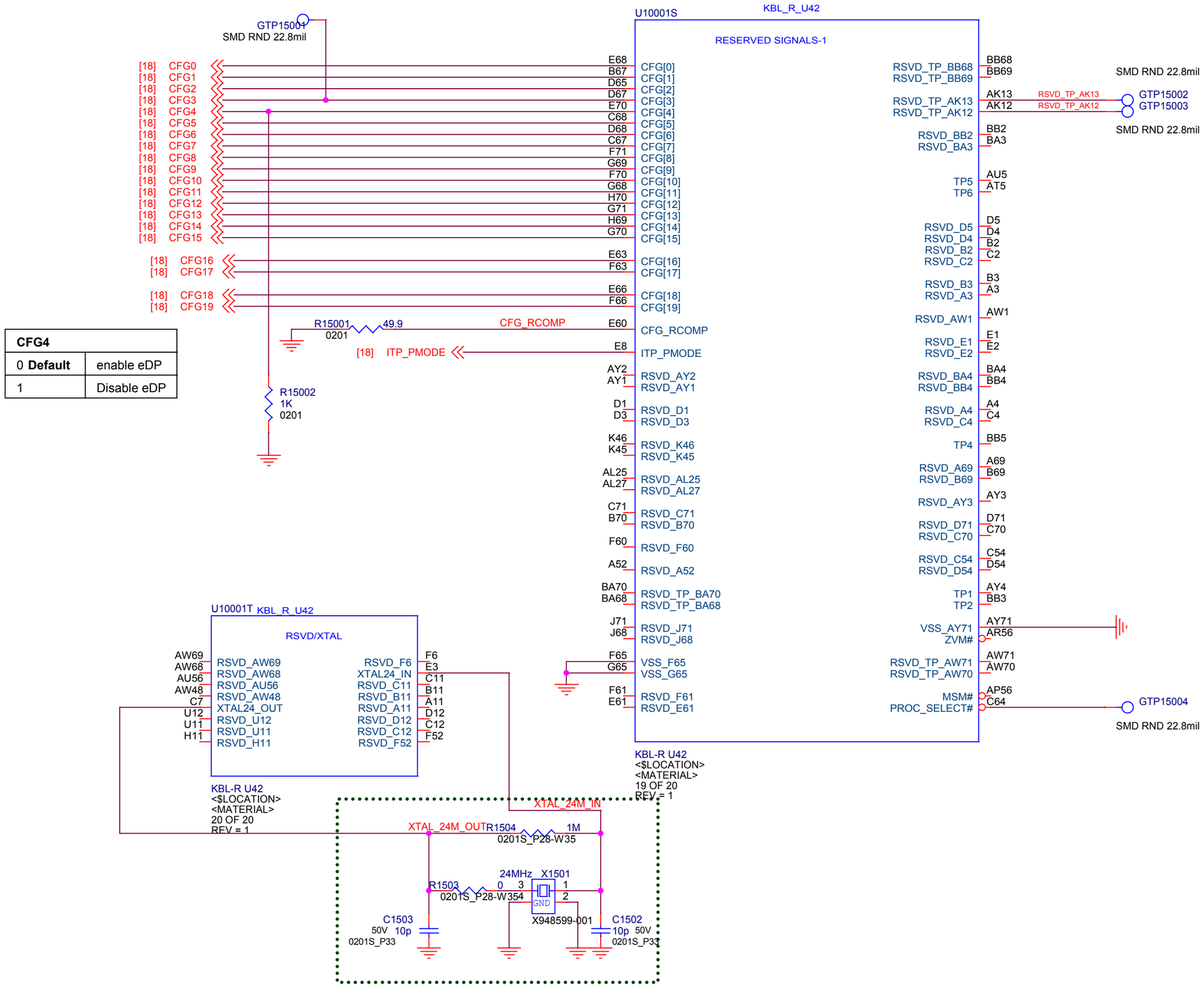
Size	Project Name	Rev
C	A	1.0.0.1

Date: Tuesday, May 01, 2018 Sheet 13 of 79



U SPECIFIC

Title:	14. CPU(5)_GND		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Friday, April 27, 2018	Sheet 14 of 79		



CFG4	
0 **Default**	enable eDP
1	Disable eDP

U SPECIFIC

Title: 15. CPU(6)_CFG_RESERVED			
Microsoft Confidential	Engineer: Surface		
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Friday, April 27, 2018	Sheet 15 of 79		

U16001
H9CCNNNBLTBLAR-NUD

U16002
H9CCNNNBLTBLAR-NUD

V0P6DX_LPDDR3

V_VREF_CA_DIMM

V_VREF_DQ_DIMM0

V1P8U_2P5U

V1P2U

GND

TBL1601

TBL1601, SEE PAGE 23

R16021 0 0603 1P8V_DUAL_VR_FB_R [58] For 1.8V sensing

R16037 0 0603 V1P2U_VR_FB_R [58] For 1.2V sensing

5 distributed. the Figure 4-56 at PDG2.0 the pink circle.

2 near each DRAM. Look the Figure 4-55 at PDG2.0 the pink circle.

5 distributed. Look the Figure 4-56 at PDG2.0 the blue circle.

3 near each DRAM. Look the Figure 4-55 at PDG2.0 the blue circle.

2 near each DRAM. Look the Figure 4-55 at PDG2.0 the red circle.

4 near each DRAM. Look the Figure 4-55 at PDG2.0 the red circle (big one).

5 distributed. Look the Figure 4-56 at PDG2.0 the red circle (VDDQ).

2 near each DRAM. Look the Figure 4-55 at PDG2.0 the yellow circle.

3 distributed. Look the Figure 4-56 at PDG2.0 the yellow circle.

DNP For 4GB System Memory: R16035, R16036

distributed along terminations. Shown in blue Figure 4-57 in PDG2.0

Edge of vtt island. Caps shown in green Figure 4-57 in PDG2.0

U SPECIFIC

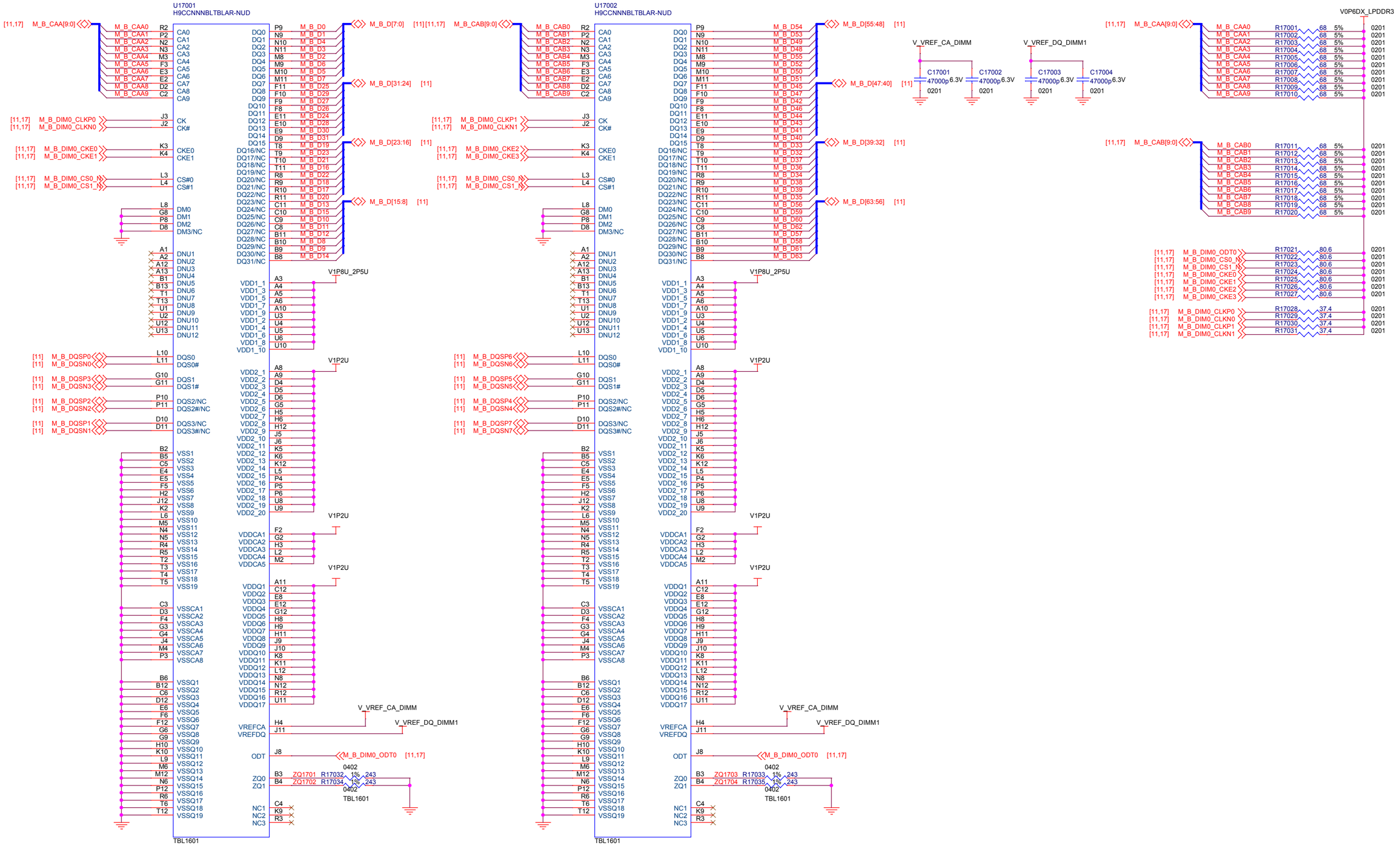
Title: 16. LPDDR3(1)_MEMORY DOWN

Microsoft Confidential

Engineer: Surface

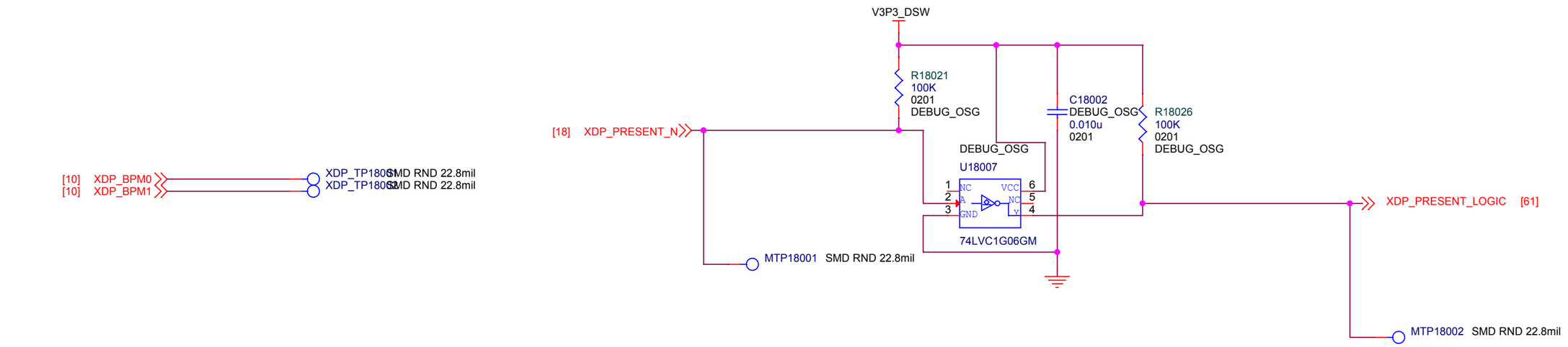
Size	Project Name	Rev
C	A	1.0.0.1

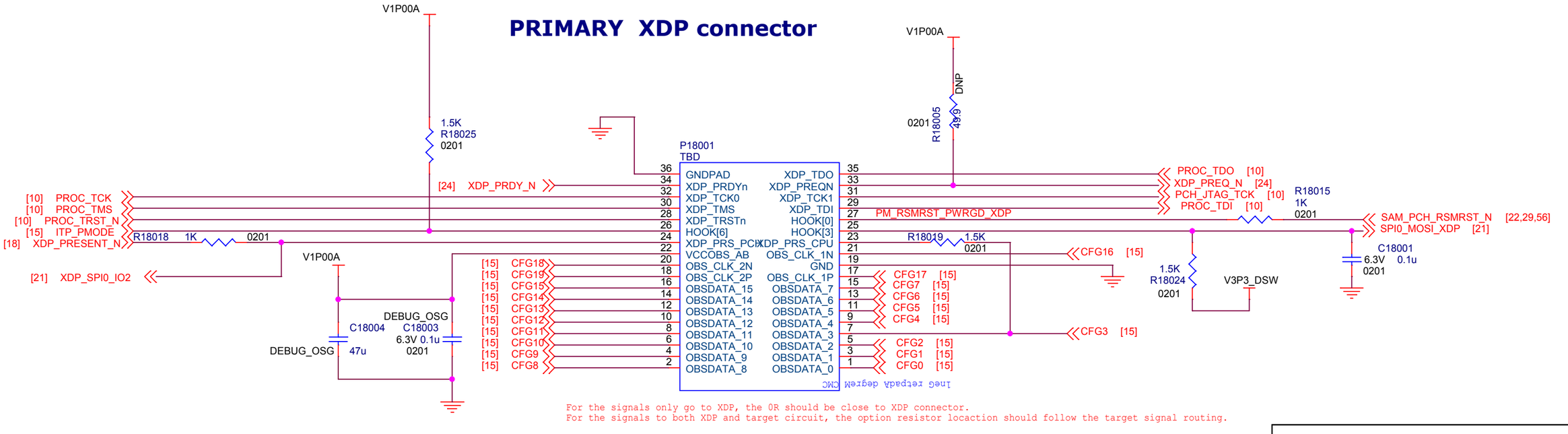
Date: Thursday, April 26, 2018 Sheet 16 of 79



U SPECIFIC

Title:	17. LPDDR3(2)_MEMORY DOWN		
Microsoft Confidential	Engineer: Surface		
Size: C	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 17 of 79		



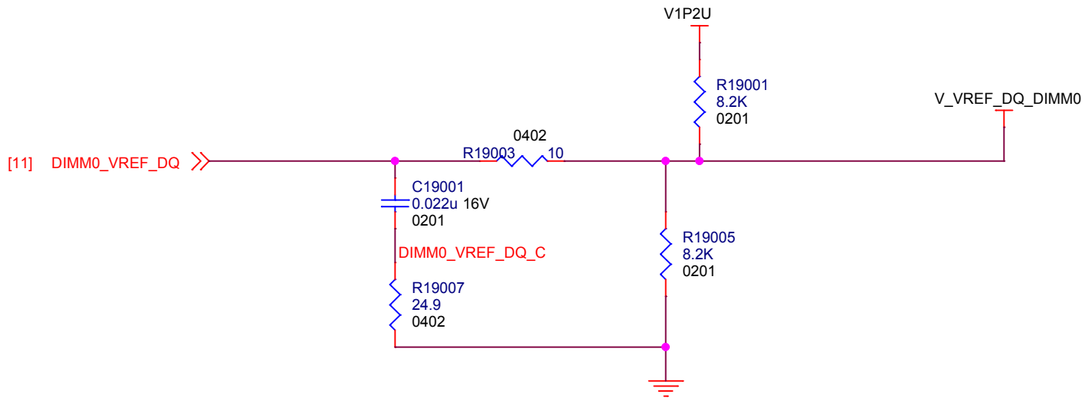


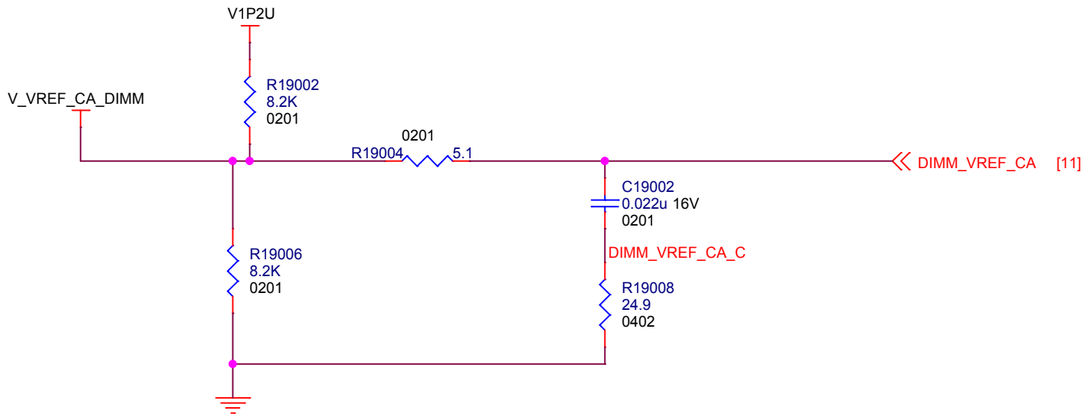
For the signals only go to XDP, the 0R should be close to XDP connector.
For the signals to both XDP and target circuit, the option resistor locaction should follow the target signal routing.

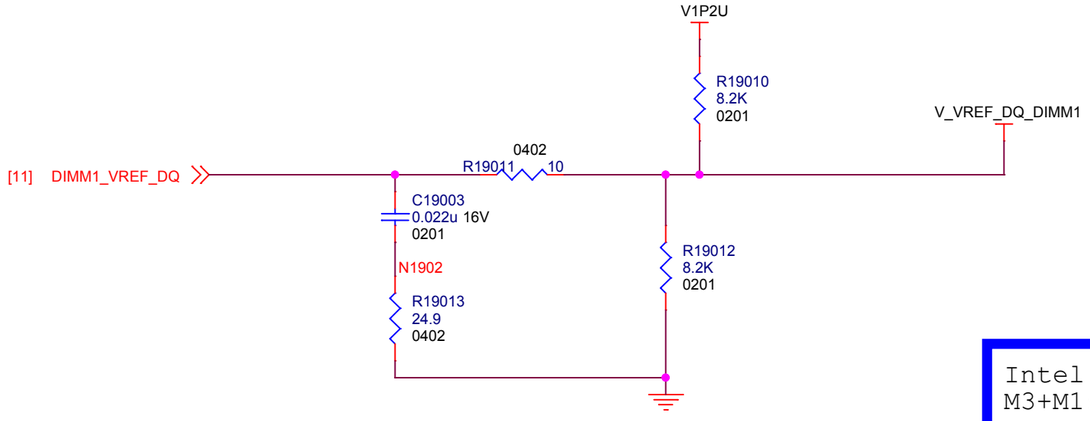
Title:	18. XDP		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 18 of 79		

LPDDR3 Vref

M3: CPU driven VREF path is stuffed by default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

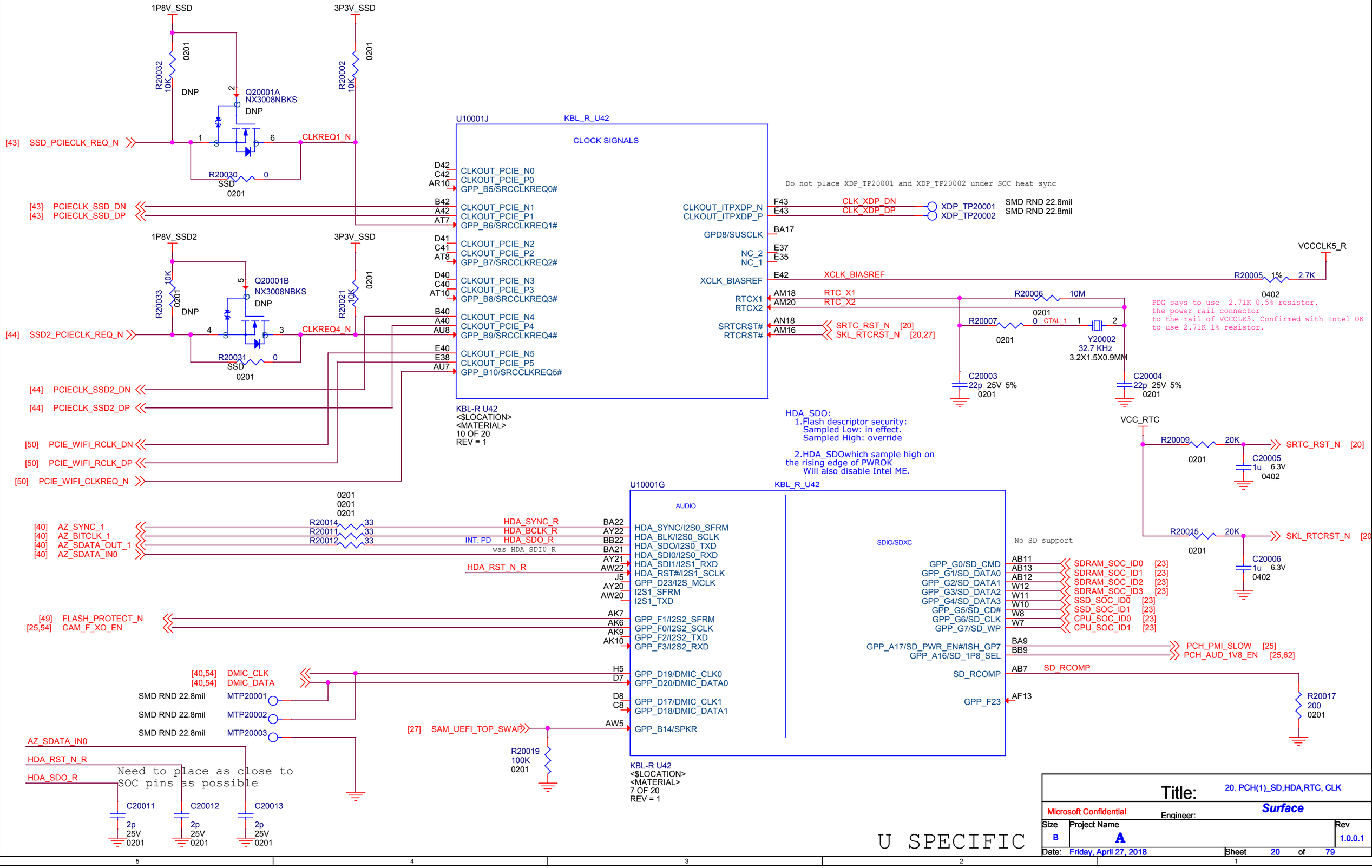






Intel 0203
M3+M1: Default Recommendation

Title:	19. LPDDR3(3)_CA/DQ Voltage	
Microsoft Confidential	Engineer: Surface	
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 19 of 79	


1P8V_SSD
3P3V_SSD
R20032 10K 0201
R20002 10K 0201
DNP
Q20001A NX3008NBKS
DNP
[43] SSD_PCIECLK_REQ_N
CLKREQ1_N
R20030 0 SSD 0201
[43] PCIECLK_SSD_DN
[43] PCIECLK_SSD_P
1P8V_SSD2
3P3V_SSD
R20033 10K 0201
R20021 10K 0201
Q20001B NX3008NBKS
DNP
[44] SSD2_PCIECLK_REQ_N
CLKREQ4_N
R20031 0 SSD 0201
[44] PCIECLK_SSD2_DN
[44] PCIECLK_SSD2_P
[50] PCIE_WIFI_RCLK_DN
[50] PCIE_WIFI_RCLK_DP
[50] PCIE_WIFI_CLKREQ_N
U10001J
KBL_R_U42
CLOCK SIGNALS
D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#
B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
AT7 GPP_B6/SRCCLKREQ1#
D41 CLKOUT_PCIE_N2
C41 CLKOUT_PCIE_P2
AT8 GPP_B7/SRCCLKREQ2#
D40 CLKOUT_PCIE_N3
C40 CLKOUT_PCIE_P3
AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
AU8 GPP_B9/SRCCLKREQ4#
E40 CLKOUT_PCIE_N5
E38 CLKOUT_PCIE_P5
AU7 GPP_B10/SRCCLKREQ5#
KBL-R U42
<$LOCATION>
<MATERIAL>
10 OF 20
REV = 1
Do not place XDP_TP20001 and XDP_TP20002 under SOC heat sync
CLKOUT_ITPXDP_N F43 CLK_XDP_DN XDP_TP20001 SMD RND 22.8mil
CLKOUT_ITPXDP_P E43 CLK_XDP_DP XDP_TP20002 SMD RND 22.8mil
GPD8/SUSCLK BA17
NC_2 E37
NC_1 E35
XCLK_BIASREF E42 XCLK_BIASREF
R20005 1% 2.7K 0402
VCCCLK5_R
RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2
R20006 10M 0201
R20007 0 CTAL_1 0201
Y20002 32.7 KHz 3.2X1.5X0.9MM
C20003 22p 25V 5% 0201
C20004 22p 25V 5% 0201
PDG says to use 2.71K 0.5% resistor.
the power rail connector
to the rail of VCCCLK5. Confirmed with Intel OK
to use 2.71K 1% resistor.
SRTCRST# AN18 SRTC_RST_N [20]
RTCRST# AM16 SKL_RTCRST_N [20,27]
HDA_SDO:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.HDA_SDOwhich sample high on
the rising edge of PWROK
Will also disable Intel ME.
VCC_RTC
R20009 20K 0201
SRTC_RST_N [20]
C20005 1u 6.3V 0402
R20015 20K 0201
SKL_RTCRST_N [20,27]
C20006 1u 6.3V 0402
U10001G
KBL_R_U42
AUDIO
0201 0201 0201
[40] AZ_SYNC_1
[40] AZ_BITCLK_1
[40] AZ_SDATA_OUT_1
[40] AZ_SDATA_IN0
R20014 33
R20011 33
R20012 33
HDA_SYNC_R BA22 HDA_SYNC/I2S0_SFRM
HDA_BCLK_R AY22 HDA_BLK/I2S0_SCLK
INT. PD HDA_SDO_R BB22 HDA_SDO/I2S0_TXD
was HDA_SDI0_R BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
HDA_RST_N_R AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD
[49] FLASH_PROTECT_N
[25,54] CAM_F_XO_EN
AK7 GPP_F1/I2S2_SFRM
AK6 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD
[40,54] DMIC_CLK
[40,54] DMIC_DATA
H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0
D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1
SMD RND 22.8mil MTP20001
SMD RND 22.8mil MTP20002
SMD RND 22.8mil MTP20003
[27] SAM_UEFI_TOP_SWAP
AW5 GPP_B14/SPKR
R20019 100K 0201
AZ_SDATA_IN0
HDA_RST_N_R
HDA_SDO_R
Need to place as close to
SOC pins as possible
C20011 2p 25V 0201
C20012 2p 25V 0201
C20013 2p 25V 0201
KBL-R U42
<$LOCATION>
<MATERIAL>
7 OF 20
REV = 1
SDIO/SDXC
No SD support
GPP_G0/SD_CMD AB11 SDRAM_SOC_ID0 [23]
GPP_G1/SD_DATA0 AB13 SDRAM_SOC_ID1 [23]
GPP_G2/SD_DATA1 AB12 SDRAM_SOC_ID2 [23]
GPP_G3/SD_DATA2 W12 SDRAM_SOC_ID3 [23]
GPP_G4/SD_DATA3 W11 SSD_SOC_ID0 [23]
GPP_G5/SD_CD# W10 SSD_SOC_ID1 [23]
GPP_G6/SD_CLK W8 CPU_SOC_ID0 [23]
GPP_G7/SD_WP W7 CPU_SOC_ID1 [23]
GPP_A17/SD_PWR_EN#/ISH_GP7 BA9 PCH_PMI_SLOW [25]
GPP_A16/SD_1P8_SEL BB9 PCH_AUD_1V8_EN [25,62]
SD_RCOMP AB7 SD_RCOMP
R20017 200 0201
GPP_F23 AF13
U SPECIFIC
Title: 20. PCH(1)_SD,HDA,RTC, CLK
Microsoft Confidential
Engineer:
Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Friday, April 27, 2018
Sheet 20 of 79

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

[18] XDP_SPI0_IO2
[18] SPI0_MOSI_XDP

R21007 1K 0201
R21008 1K 0201

Close to PCH

[37] SPI_CLK
[37] SPI_SO
[37] SPI_SI
[37] SPI_WP_IO2
[37] SPI_HOLD_IO3_N
[37] SPI_CS0_N

R21011 15 0201 SPI_CLK_R
R21012 15 0201 SPI_SO_R
R21013 15 0201 SPI_SI_R
R21009 15 0201 SPI_WP_IO2_R
R21010 15 0201 SPI_HOLD_IO3_R_N
R21023 15 0201

[49] TS_SPI_CLK
[49] TS_SPI_MISO
[49] TS_SPI_MOSI

R21014 15 0201 TS_SPI_CLK_R
R21015 15 0201 TS_SPI_MISO_R
R21016 15 0201 TS_SPI_MOSI_R

[49] TS_SPI_CS_N

R21019 15 0201 TS_SPI_CS_N_R

3VSUS_ORG

R21029 10K 1% 0201

U10001E

KBL_R_U42

SPI - FLASH

SPI0_CLK AV2
SPI0_MISO AW3
SPI0_MOSI AV3
SPI0_IO2 AW2
SPI0_IO3 AU4
SPI0_CS0# AU3
SPI0_CS1# AU2
SPI0_CS2# AU1

SPI_TOUCH

GPP_D1/SPI1_CLK M2
GPP_D2/SPI1_MISO M3
GPP_D3/SPI1_MOSI J4
GPP_D21/SPI1_IO2 V1
GPP_D22/SPI1_IO3 V2
GPP_D0/SPI1_CS# M1

C LINK

CL_CLK G3
CL_DATA G2
CL_RST# G1

GPP_A0/RCIN# AW13
GPP_A6/SERIRQ AY11

SMBUS, SMLINK 1

GPP_C0/SMBCLK R7
GPP_C1/SMBDATA R8
GPP_C2/SMBALERT# R10 INT. PD

GPP_C3/SML0CLK R9
GPP_C4/SML0DATA W2
GPP_C5/SML0ALERT# W1 INT. PD was SMB0ALERT#

GPP_C5 - LPC boot mode selection - needs to be 0

GTP21013 SMD RND 22.8mil

GPP_C6/SML1CLK W3
GPP_C7/SML1DATA V3
GPP_B23/SML1ALERT#/PCHHOT# AM7 INT. PD

R21004 10K 1% 0201
R21031 100K 1% 0201

LPC

GPP_A1/LAD0/ESPI_IO0 AY13
GPP_A2/LAD1/ESPI_IO1 BA13
GPP_A3/LAD2/ESPI_IO2 BB13
GPP_A4/LAD3/ESPI_IO3 AY12
GPP_A5/LFRAME#/ESPI_CS# BA12
GPP_A14/SUS_STAT#/ESPI_RESET# BA11

TPM_LPC0 [38]
TPM_LPC1 [38]
TPM_LPC2 [38]
TPM_LPC3 [38]
TPM_LFRAME [38]
TPM_DEEPSLP_N [38]

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9
GPP_A10/CLKOUT_LPC1 AY9
GPP_A8/CLKRUN# AW11

CK_24M_EC_R
R21020 22 0201
TPM_CLK [38]

C21002 10p 50V 0201 DNP

3VSUS_ORG
R21021 8.2K 0201
TPM_CLKRUN [38]

KBL-R U42
<$LOCATION>
<MATERIAL>
5 OF 20
REV = 1

[38] TPM_SERIRQ
Serial Interrupt Request

Need into improve LPC signals - P had in their latest design

GPP_C2/SMBALERT#	
0 **Default**	Disable ME crypto TLS
1	Enable ME crypto TLS

Needs to be left open or low for booting

R21024	49.9	0201	LAD0_SKL_TERM
R21027	49.9	0201	LAD1_SKL_TERM
R21025	49.9	0201	LAD2_SKL_TERM
R21026	49.9	0201	LAD3_SKL_TERM

C21003	56p	25V	0201
C21006	56p	25V	0201
C21004	56p	25V	0201
C21005	56p	25V	0201

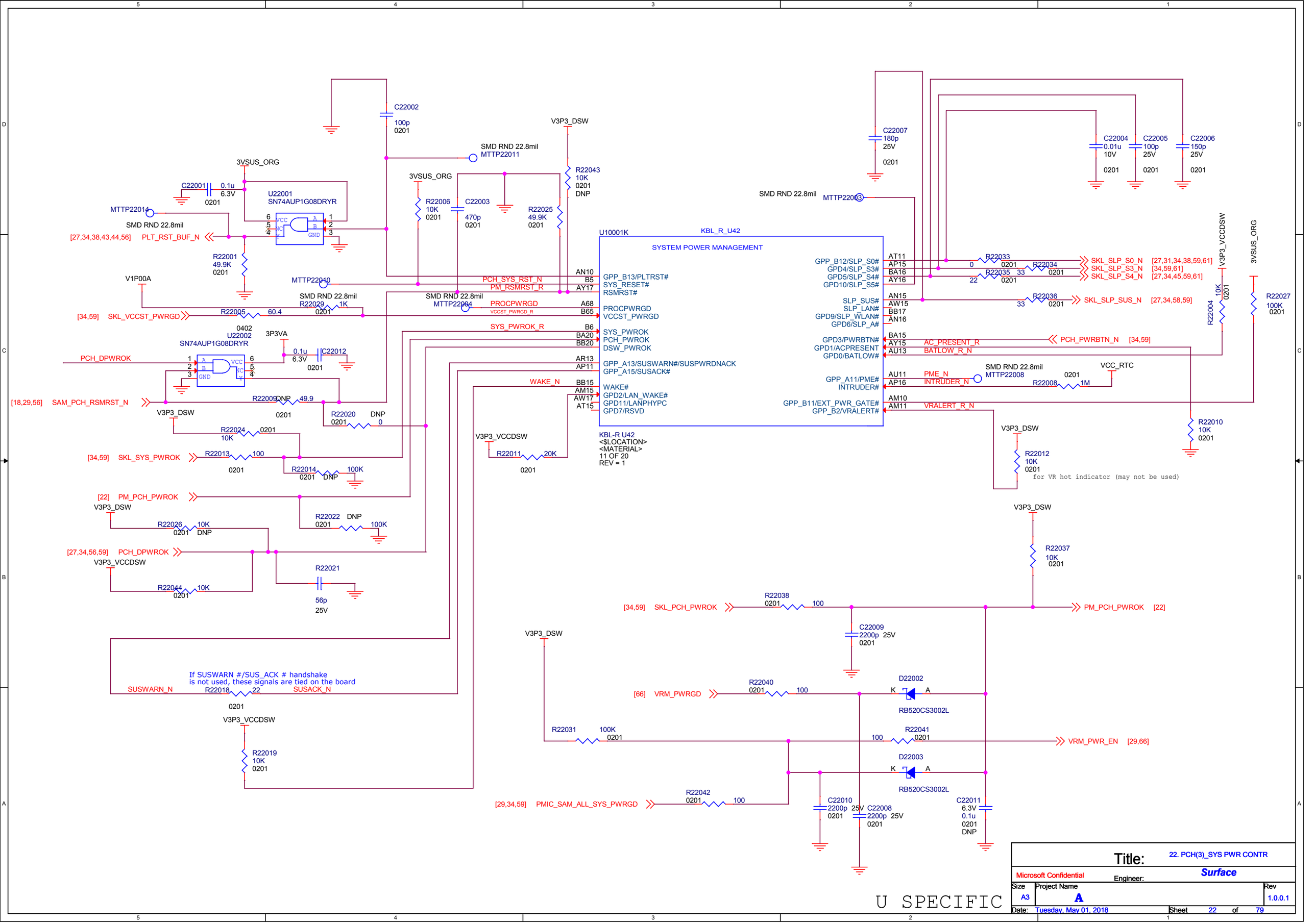
U SPECIFIC

Title: 21. PCH(2)_CLK,SMB,LPC, SPI

Microsoft Confidential Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Friday, April 27, 2018 Sheet 21 of 79



U SPECIFIC

Title:	22. PCH(3)_SYS PWR CONTR	
Microsoft Confidential	Engineer:	Surface
Size: A3	Project Name: A	Rev: 1.0.0.1
Date: Tuesday, May 01, 2018	Sheet 22 of 79	

TBL2301B

R23016, R28013 LOAD FOR DEBUG, ELSE NO-STUFF

R23023, R28024 LOAD FOR RETAIL, ELSE NO-STUFF

TBL2301A

R23015, R28014 NEW BOARDID SYSTEM, ELSE NO-STUFF

R23022, R28025 OLD BOARDID SYSTEM, ELSE NO-STUFF

TBL2301 PCBA vendor and revision

R23010, R23020, R23024	Revision EV2P5
R23005, R23013, R23017, R28051, R28052, R28053	NO-STUFF FOR REVISION
R23005, R23020, R23024, R28051	Revision EV2P51
R23010, R23013, R23017, R28052, R28053	NO-STUFF FOR REVISION
R23010, R23013, R23024, R28052	Revision DV
R23005, R23020, R23017, R28051, R28053	NO-STUFF FOR REVISION
R23005, R23013, R23024, R28051, R28052	Revision DV1.01
R23010, R23020, R23017, R28053	NO-STUFF FOR REVISION
R23010, R23020, R23017, R28053	Revision DV1.1, DV1.2, PV
R23005, R23013, R23024, R28051, R28052	NO-STUFF FOR REVISION
R23005, R23020, R23017, R28051, R28053	Lacey EV1
R23010, R23013, R23024, R28052	NO-STUFF FOR REVISION
R23010, R23013, R23017, R28052, R28053	Reserved
R23005, R23020, R23024, R28051	NO-STUFF FOR REVISION
R23005, R23013, R23017, R28051, R28052, R28053	Reserved
R23010, R23020, R23024	NO-STUFF FOR REVISION

TBL_SSD_2302

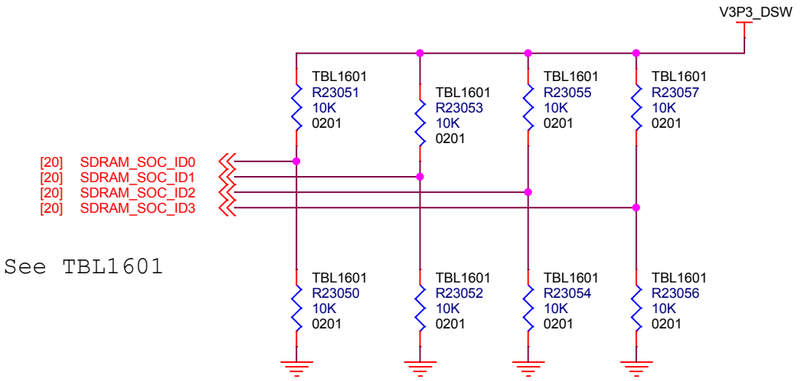
BoardID	SSD vendor	stuff	No-Stuff
00	Toshiba SSD	R23030, R23032	R23031, R23033, R28081, R28082
01	SAMSUNG SSD	R23031, R23032, R28081	R23030, R23033, R28082
10	INTEL PS SSD	R23030, R23033, R28082	R23031, R23032, R28081
11	Hynix SSD	R23031, R23033, R28081, R28082	R23030, R23032

TBL2304

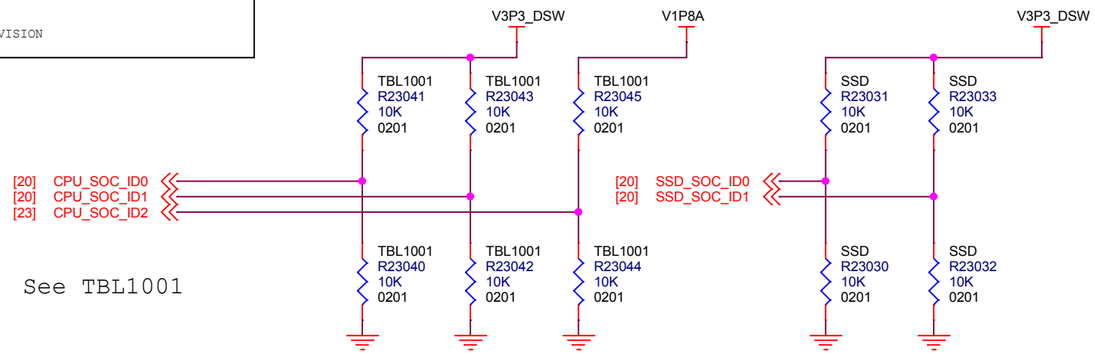
BoardID	GreenPak Revision	stuff	No-Stuff
00	Initial release, Mxxxxxx-001	R23008, R23009	R23003, R23004, R28061, R28062
01	1st new revision	R23003, R23009, R28061	R23008, R23004, R28062
10	2nd new revision	R23008, R23004, R28062	R23003, R23009, R28061
11	3rd new revision	R23003, R23004, R28061, R28062	R23008, R23009

TBL1601

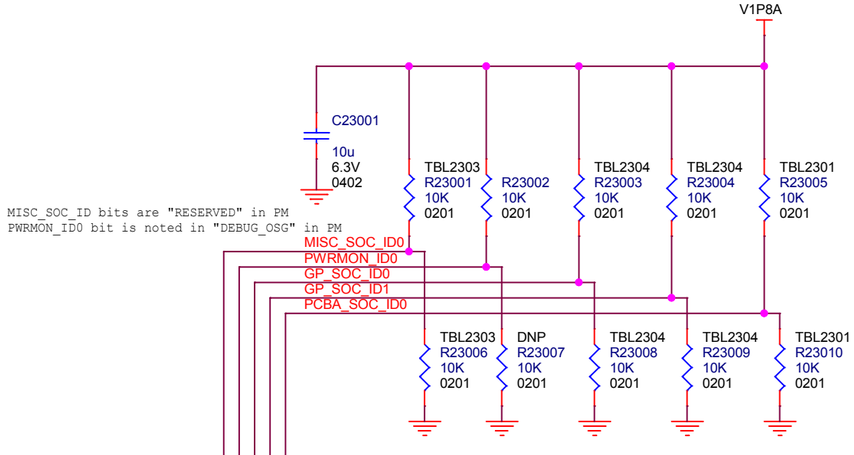
BoardID	sdram vendor and revision	Size	stuff	No-Stuff
0000	Hynix: H9CCNNN8JTBLAR-NUD, 8Gb LPDDR3	4GB	R23050, R23052, R23054, R2305	R23051, R23053, R23055, R23057
0001	Samsung: K4E8E324EB-EGCF000, 8Gb LPDDR3	4GB	R23051, R23052, R23054, R2305	R23050, R23053, R23055, R23057
0010	Hynix: H9CCNNN8GTALAR-NUD, 8gB LPDDR3	4GB	R23050, R23053, R23054, R2305	R23051, R23052, R23055, R23057
0011	Reserved	4GB	R23051, R23053, R23054, R2305	R23050, R23052, R23055, R23057
0100	Hynix: H9CCNNNBLTBLAR-NUD, 16Gb LPDDR3	8GB	R23050, R23052, R23055, R2305	R23051, R23053, R23054, R23057
0101	Samsung: K4E6E304EB-EGCF000, 16Gb LPDDR3	8GB	R23051, R23052, R23055, R2305	R23050, R23053, R23054, R23057
0110	Hynix: H9CCNNNBJTALAR-NUD, 16Gb LPDDR3	8GB	R23050, R23053, R23055, R2305	R23051, R23052, R23054, R23057
0111	Reserved	8GB	R23051, R23053, R23055, R2305	R23050, R23052, R23054, R23057
1000	Hynix: H9CCNNNCLTMLBR-NUD, 32Gb LPDDR3	16GB	R23050, R23052, R23054, R2305	R23051, R23053, R23055, R23056
1001	Samsung: K4EBE304EB-EGCF000, 32Gb LPDDR3	16GB	R23051, R23052, R23054, R2305	R23050, R23053, R23055, R23056
1010	Hynix: H9CCNNNCLGALAR-NUD, 32Gb LPDDR3	16GB	R23050, R23053, R23054, R2305	R23051, R23052, R23055, R23056
1011	Reserved	16GB	R23051, R23053, R23054, R2305	R23050, R23052, R23055, R23056
1100	Reserved	Reserved	R23050, R23052, R23055, R2305	R23051, R23053, R23054, R23056
1101	Reserved	Reserved	R23051, R23052, R23055, R2305	R23050, R23053, R23054, R23056
1110	Reserved	Reserved	R23050, R23053, R23055, R2305	R23051, R23052, R23054, R23056
1111	Reserved	Reserved	R23051, R23053, R23055, R2305	R23050, R23052, R23054, R23056

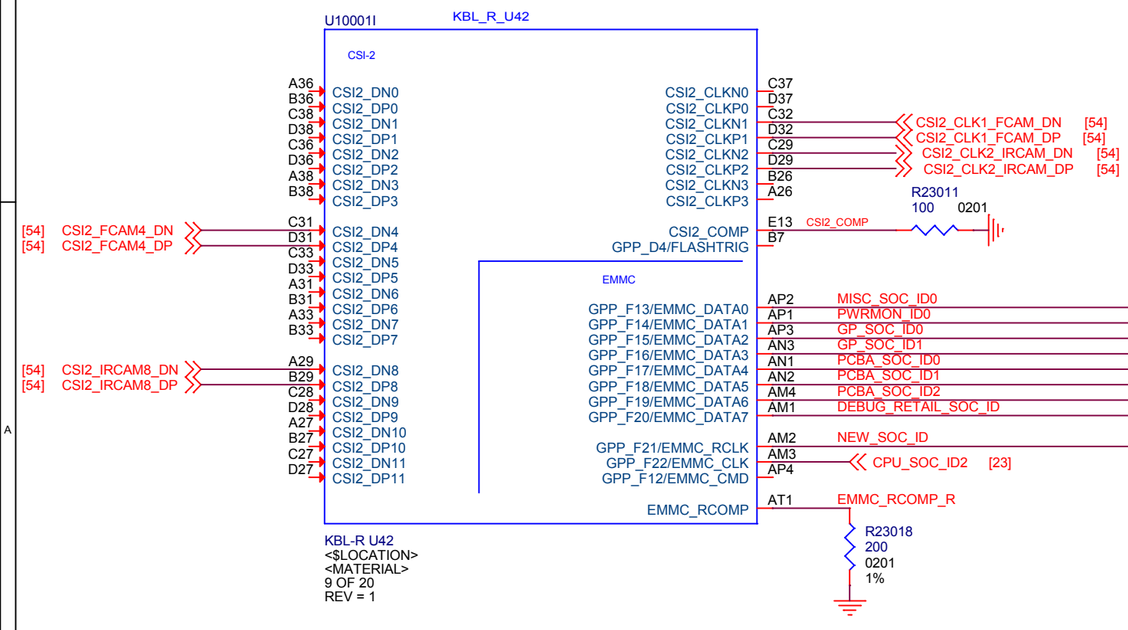


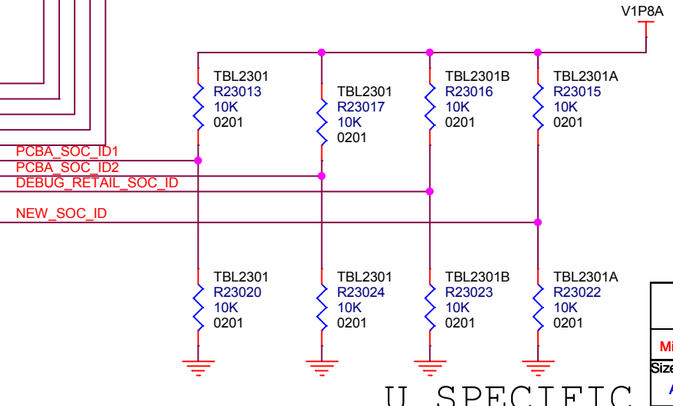
See TBL1601



See TBL1001







POWER MONITORS

R23007 POWER MONITORS, ELSE NO-STUFF

R23002 NO POWER MONITORS, ELSE NO-STUFF

DV HAS NO POWER MONITORS

U SPECIFIC

Microsoft Confidential

Title: 23. PCH(4)_CCI, HWID

Engineer:

Surface

Size	Project Name	Rev
A3	A	1.0.0.1

Date: Friday, April 27, 2018 Sheet 23 of 79

U10001H

KBL_R_U42

PCIE/USB3/SATA

SSIC / USB3

USB2

H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP

G11 PCIE2_RXN/USB3_6_RXN
F11 PCIE2_RXP/USB3_6_RXP
D16 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP

H16 PCIE3_RXN
G16 PCIE3_RXP
D17 PCIE3_TXN
C17 PCIE3_TXP

G15 PCIE4_RXN
F15 PCIE4_RXP
B19 PCIE4_TXN
A19 PCIE4_TXP

F16 PCIE5_RXN
E16 PCIE5_RXP
C19 PCIE5_TXN
D19 PCIE5_TXP

G18 PCIE6_RXN
F18 PCIE6_RXP
D20 PCIE6_TXN
C20 PCIE6_TXP

F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP

G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP

E22 PCIE9_RXN
E23 PCIE9_RXP
B23 PCIE9_TXN
A23 PCIE9_TXP

F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP

F5 PCIE_RCOMP_N
E5 PCIE_RCOMP_P

D56 PROC_PRDY#
D61 PROC_PREQ#
BB11 GPP_A7/PIRQA#

E28 PCIE11_RXN/SATA1B_RXN
E27 PCIE11_RXP/SATA1B_RXP
D24 PCIE11_TXN/SATA1B_TXN
C24 PCIE11_TXP/SATA1B_TXP
E30 PCIE12_RXN/SATA2_RXN
F30 PCIE12_RXP/SATA2_RXP
A25 PCIE12_TXN/SATA2_TXN
B25 PCIE12_TXP/SATA2_TXP

H8 USB3_1_RXN
G8 USB3_1_RXP
C13 USB3_1_TXN
D13 USB3_1_TXP

J6 USB3_2_RXN/SSIC_RXN
H6 USB3_2_RXP/SSIC_RXP
B13 USB3_2_TXN/SSIC_TXN
A13 USB3_2_TXP/SSIC_TXP

J10 USB3_3_RXN
H10 USB3_3_RXP
B15 USB3_3_TXN
A15 USB3_3_TXP

E10 USB3_4_RXN
F10 USB3_4_RXP
C15 USB3_4_TXN
D15 USB3_4_TXP

AB9 USB2N_1
AB10 USB2P_1
AD6 USB2N_2
AD7 USB2P_2
AH3 USB2N_3
AJ3 USB2P_3
AD9 USB2N_4
AD10 USB2P_4
AJ1 USB2N_5
AJ2 USB2P_5
AF6 USB2N_6
AF7 USB2P_6
AH1 USB2N_7
AH2 USB2P_7
AF8 USB2N_8
AF9 USB2P_8
AG1 USB2N_9
AG2 USB2P_9
AH7 USB2N_10
AH8 USB2P_10

AB6 USB2_COMP
AG3 USB2_ID
AG4 USB2_VBUSSENSE

A9 GPP_E9/USB2_OC0#
C9 GPP_E10/USB2_OC1#
D9 GPP_E11/USB2_OC2#
B9 GPP_E12/USB2_OC3#

J1 GPP_E4/DEVSLP0
J2 GPP_E5/DEVSLP1
J3 GPP_E6/DEVSLP2

H2 GPP_E0/SATAXPCIE0/SATAGP0
H3 GPP_E1/SATAXPCIE1/SATAGP1
G4 GPP_E2/SATAXPCIE2/SATAGP2

H1 GPP_E8/SATALED#

USB Type A
USB3_TYPEA_RX_DN [45]
USB3_TYPEA_RX_DP [45]
USB3_TYPEA_TX_DN [45]
USB3_TYPEA_TX_DP [45]

USB3 SL1
USB3_SL_RX_DN [47]
USB3_SL_RX_DP [47]
USB3_SL_TX_DN [47]
USB3_SL_TX_DP [47]

C24031 10p 0201
C24032 10p 0201

USB Type A
USB2_TYPEA_DN [45]
USB2_TYPEA_DP [45]

USB2 SL1
USB2_SL_DN [47]
USB2_SL_DP [47]

BT
USB2_BT_DN [50]
USB2_BT_DP [50]

USB2_COMP 0201 R24004 113
R24005 0201 10K
3VSUS_ORG
USB_CONN_OC_N [45]
0201 C24030 10p
GND

SSD2_SATA_PCIE_DET_N [44]

PCIE SSD1

[43] PCIE_SSD_RX7_DN
[43] PCIE_SSD_RX7_DP
[43] PCIE_SSD_TX7_DN
[43] PCIE_SSD_TX7_DP
C24003 0.22u SSD 0201 6.3V
C24004 SSD 0.22u 0201 6.3V 0201

[43] PCIE_SSD_RX8_DN
[43] PCIE_SSD_RX8_DP
[43] PCIE_SSD_TX8_DN
[43] PCIE_SSD_TX8_DP
C24005 0.22u SSD 0201 6.3V
C24006 SSD 0.22u 0201 6.3V 0201

PCIE WIFI

[50] PCIE_WIFI_RX9_DN
[50] PCIE_WIFI_RX9_DP
[50] PCIE_WIFI_TX9_DN
[50] PCIE_WIFI_TX9_DP
C24007 0.1u 6.3V 0201
C24008 0.1u 0201 6.3V

3VSUS_ORG
R24009 10K 1% 0201

PCIE_RCOMPN
PCIE_RCOMPP
R24006 100 0201

[18] XDP_PRDY_N
[18] XDP_PREQ_N
PIRQA_N

PCIE SSD2

[44] PCIE_SSD2_RX11_DN
[44] PCIE_SSD2_RX11_DP
[44] PCIE_SSD2_TX11_DN
[44] PCIE_SSD2_TX11_DP
[44] PCIE_SSD2_RX12_DN
[44] PCIE_SSD2_RX12_DP
[44] PCIE_SSD2_TX12_DN
[44] PCIE_SSD2_TX12_DP
0.22u 0201 6.3V C24020 SSD 0.22u 0201 6.3V C24021 SSD
0.22u 0201 6.3V C24022 SSD 0.22u 0201 6.3V C24023 SSD

KBL-R U42
<$LOCATION>
<MATERIAL>
8 OF 20
REV = 1

U SPECIFIC

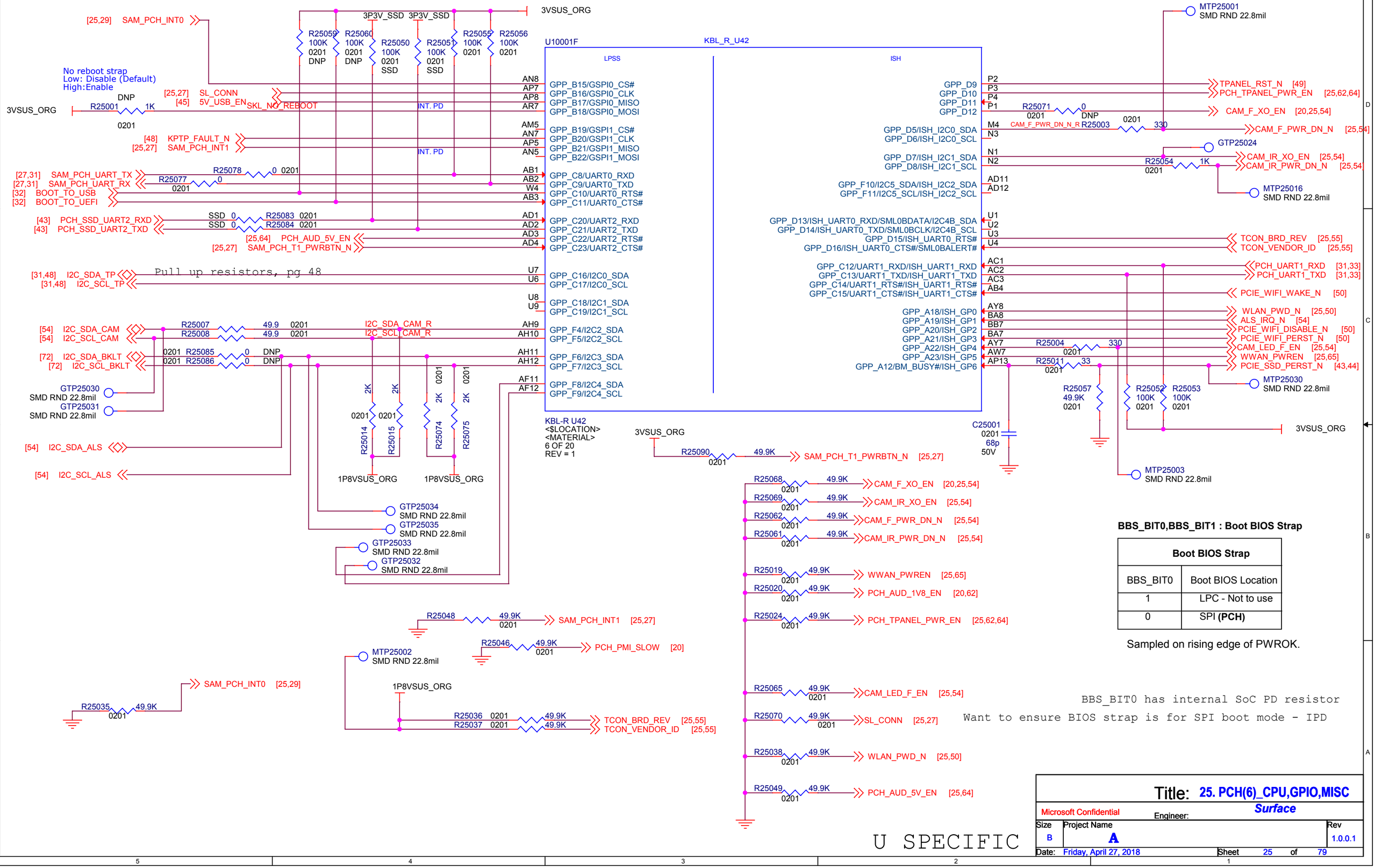
Title: 24. PCH(5)_PCIE,USB

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
A3	A	1.0.0.1

Date: Friday, April 27, 2018 Sheet 24 of 79



BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap	
BBS_BIT0	Boot BIOS Location
1	LPC - Not to use
0	SPI **(PCH)**

Sampled on rising edge of PWROK.

BBS_BIT0 has internal SoC PD resistor

Want to ensure BIOS strap is for SPI boot mode - IPD

U SPECIFIC

Title:	25. PCH(6)_CPU,GPIO,MISC		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Friday, April 27, 2018	Sheet 25 of 79		

Put this logic at near SOC VCCPRIM.

U10001O KBL_R_U42

CPU POWER 4 OF 4

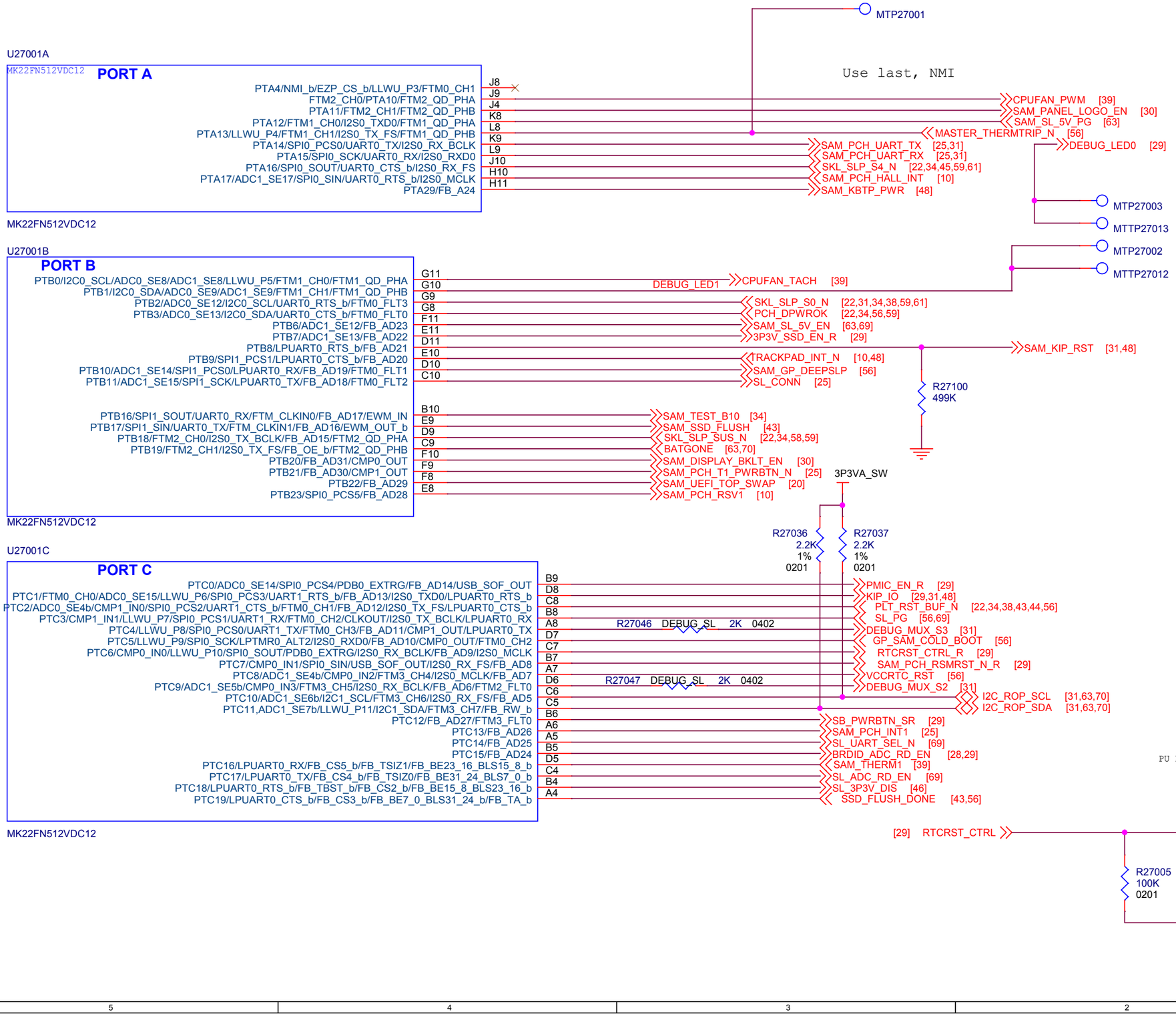
KBL-R U42
<$LOCATION>
<MATERIAL>
15 OF 20
REV = 1

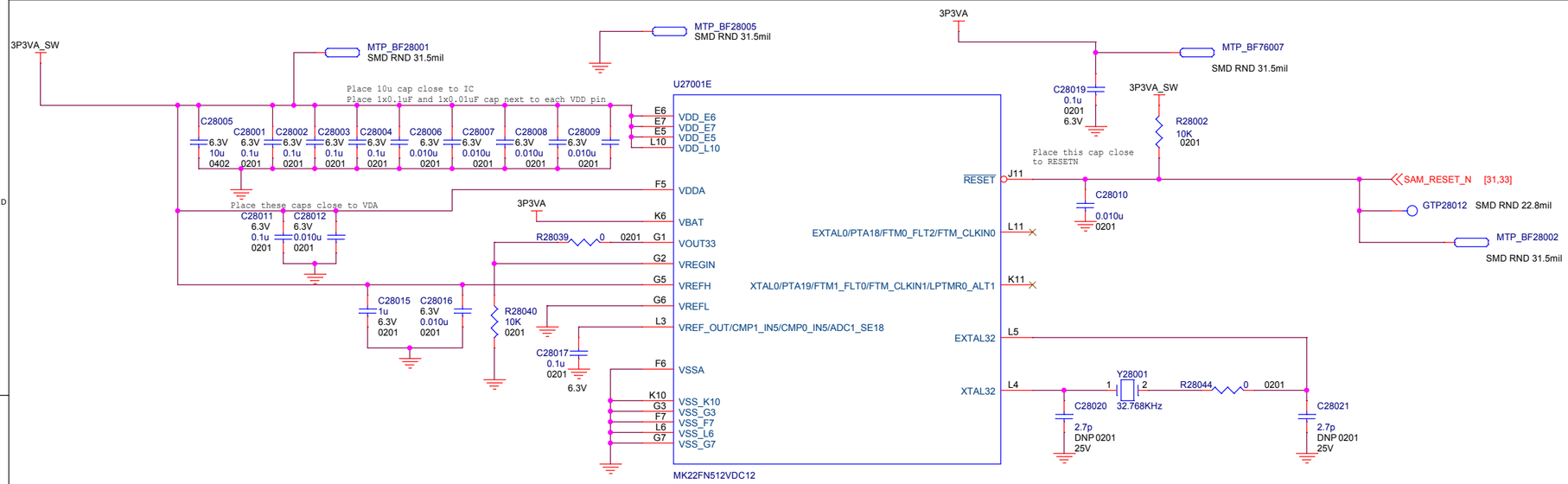
VCCPLL(VCCSFR)=0.12A

2pF caps need to be place as close to SOC pins as possible

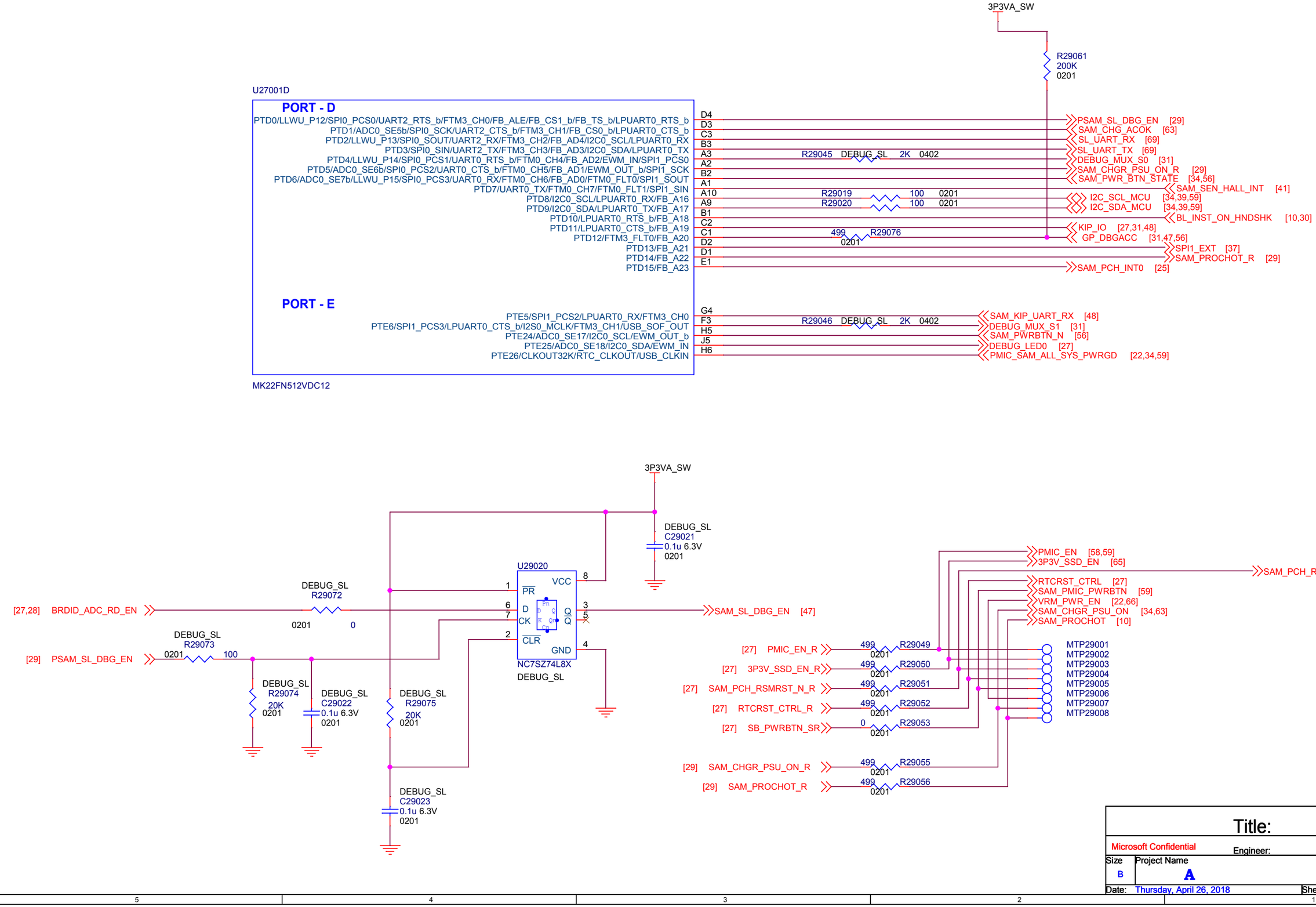
U SPECIFIC

Title:	26. PCH(7)_POWER		
Microsoft Confidential	Engineer:	Surface	
Size: A3	Project Name: A		Rev: 1.0.0.1
Date: Friday, April 27, 2018	Sheet 26 of 79		

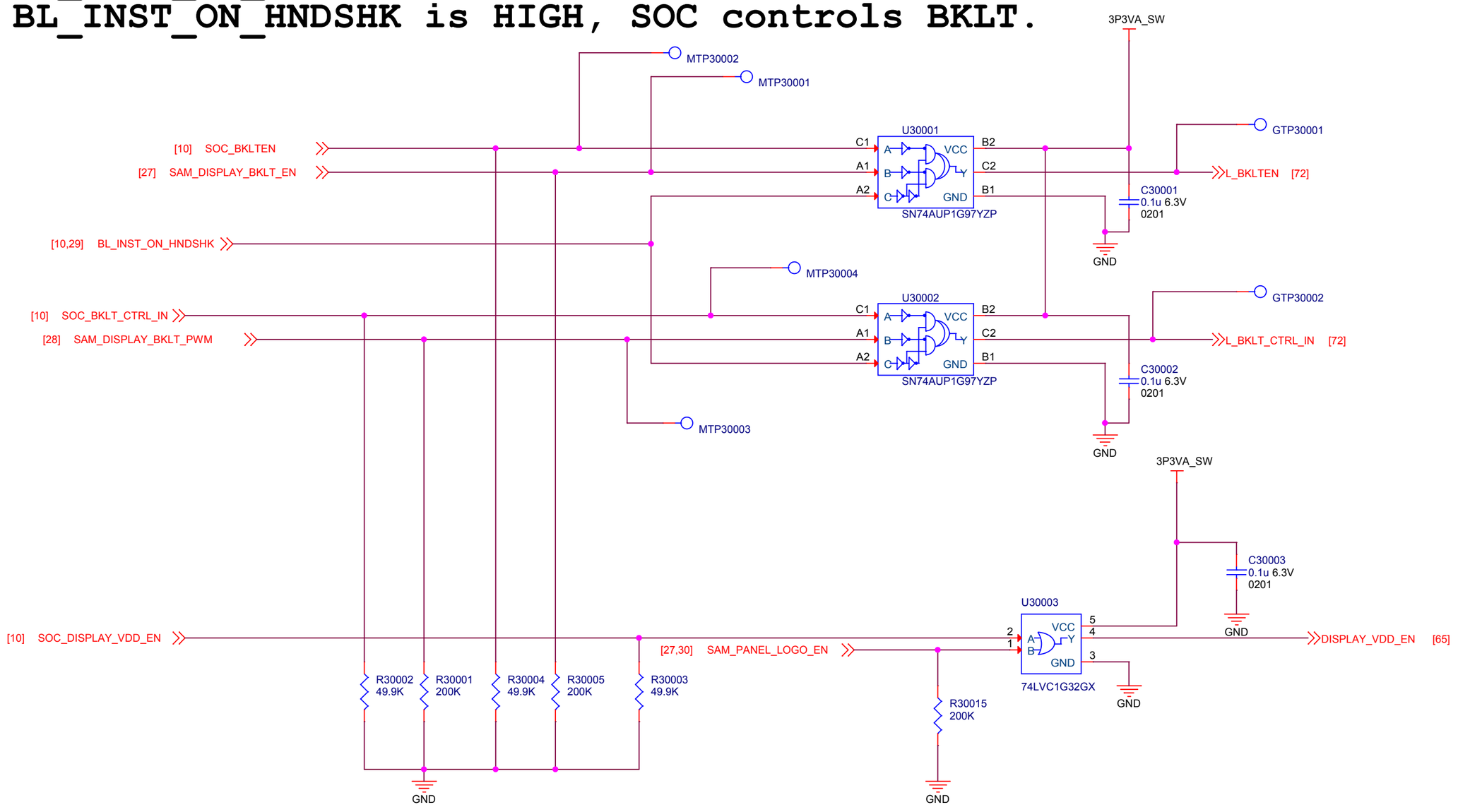

U27001A
MK22FN512VDC12
PORT A
PTA4/NMI_b/EZP_CS_b/LLWU_P3/FTM0_CH1
FTM2_CH0/PTA10/FTM2_QD_PHA
PTA11/FTM2_CH1/FTM2_QD_PHB
PTA12/FTM1_CH0/I2S0_TXD0/FTM1_QD_PHA
PTA13/LLWU_P4/FTM1_CH1/I2S0_TX_FS/FTM1_QD_PHB
PTA14/SPI0_PCS0/UART0_TX/I2S0_RX_BCLK
PTA15/SPI0_SCK/UART0_RX/I2S0_RXD0
PTA16/SPI0_SOUT/UART0_CTS_b/I2S0_RX_FS
PTA17/ADC1_SE17/SPI0_SIN/UART0_RTS_b/I2S0_MCLK
PTA29/FB_A24
J8
J9
J4
K8
L8
K9
L9
J10
H10
H11
MTP27001
Use last, NMI
CPUFAN_PWM [39]
SAM_PANEL_LOGO_EN [30]
SAM_SL_5V_PG [63]
MASTER_THERMTRIP_N [56]
SAM_PCH_UART_TX [25,31]
SAM_PCH_UART_RX [25,31]
SKL_SLP_S4_N [22,34,45,59,61]
SAM_PCH_HALL_INT [10]
SAM_KBTP_PWR [48]
DEBUG_LED0 [29]
MTP27003
MTTP27013
MK22FN512VDC12
U27001B
PORT B
PTB0/I2C0_SCL/ADC0_SE8/ADC1_SE8/LLWU_P5/FTM1_CH0/FTM1_QD_PHA
PTB1/I2C0_SDA/ADC0_SE9/ADC1_SE9/FTM1_CH1/FTM1_QD_PHB
PTB2/ADC0_SE12/I2C0_SCL/UART0_RTS_b/FTM0_FLT3
PTB3/ADC0_SE13/I2C0_SDA/UART0_CTS_b/FTM0_FLT0
PTB6/ADC1_SE12/FB_AD23
PTB7/ADC1_SE13/FB_AD22
PTB8/LPUART0_RTS_b/FB_AD21
PTB9/SPI1_PCS1/LPUART0_CTS_b/FB_AD20
PTB10/ADC1_SE14/SPI1_PCS0/LPUART0_RX/FB_AD19/FTM0_FLT1
PTB11/ADC1_SE15/SPI1_SCK/LPUART0_TX/FB_AD18/FTM0_FLT2
PTB16/SPI1_SOUT/UART0_RX/FTM_CLKIN0/FB_AD17/EWM_IN
PTB17/SPI1_SIN/UART0_TX/FTM_CLKIN1/FB_AD16/EWM_OUT_b
PTB18/FTM2_CH0/I2S0_TX_BCLK/FB_AD15/FTM2_QD_PHA
PTB19/FTM2_CH1/I2S0_TX_FS/FB_OE_b/FTM2_QD_PHB
PTB20/FB_AD31/CMP0_OUT
PTB21/FB_AD30/CMP1_OUT
PTB22/FB_AD29
PTB23/SPI0_PCS5/FB_AD28
G11
G10
G9
G8
F11
E11
D11
E10
D10
C10
B10
E9
D9
C9
F10
F9
F8
E8
DEBUG_LED1
CPUFAN_TACH [39]
MTP27002
MTTP27012
SKL_SLP_S0_N [22,31,34,38,59,61]
PCH_DPWROK [22,34,56,59]
SAM_SL_5V_EN [63,69]
3P3V_SSD_EN_R [29]
TRACKPAD_INT_N [10,48]
SAM_GP_DEEPSLP [56]
SL_CONN [25]
SAM_KIP_RST [31,48]
R27100
499K
SAM_TEST_B10 [34]
SAM_SSD_FLUSH [43]
SKL_SLP_SUS_N [22,34,58,59]
BATGONE [63,70]
SAM_DISPLAY_BKLT_EN [30]
SAM_PCH_T1_PWRBTN_N [25]
SAM_UEFI_TOP_SWAP [20]
SAM_PCH_RSV1 [10]
3P3VA_SW
R27036
2.2K
1%
0201
R27037
2.2K
1%
0201
MK22FN512VDC12
U27001C
PORT C
PTC0/ADC0_SE14/SPI0_PCS4/PDB0_EXTRG/FB_AD14/USB_SOF_OUT
PTC1/FTM0_CH0/ADC0_SE15/LLWU_P6/SPI0_PCS3/UART1_RTS_b/FB_AD13/I2S0_TXD0/LPUART0_RTS_b
PTC2/ADC0_SE4b/CMP1_IN0/SPI0_PCS2/UART1_CTS_b/FTM0_CH1/FB_AD12/I2S0_TX_FS/LPUART0_CTS_b
PTC3/CMP1_IN1/LLWU_P7/SPI0_PCS1/UART1_RX/FTM0_CH2/CLKOUT/I2S0_TX_BCLK/LPUART0_RX
PTC4/LLWU_P8/SPI0_PCS0/UART1_TX/FTM0_CH3/FB_AD11/CMP1_OUT/LPUART0_TX
PTC5/LLWU_P9/SPI0_SCK/LPTMR0_ALT2/I2S0_RXD0/FB_AD10/CMP0_OUT/FTM0_CH2
PTC6/CMP0_IN0/LLWU_P10/SPI0_SOUT/PDB0_EXTRG/I2S0_RX_BCLK/FB_AD9/I2S0_MCLK
PTC7/CMP0_IN1/SPI0_SIN/USB_SOF_OUT/I2S0_RX_FS/FB_AD8
PTC8/ADC1_SE4b/CMP0_IN2/FTM3_CH4/I2S0_MCLK/FB_AD7
PTC9/ADC1_SE5b/CMP0_IN3/FTM3_CH5/I2S0_RX_BCLK/FB_AD6/FTM2_FLT0
PTC10/ADC1_SE6b/I2C1_SCL/FTM3_CH6/I2S0_RX_FS/FB_AD5
PTC11,ADC1_SE7b/LLWU_P11/I2C1_SDA/FTM3_CH7/FB_RW_b
PTC12/FB_AD27/FTM3_FLT0
PTC13/FB_AD26
PTC14/FB_AD25
PTC15/FB_AD24
PTC16/LPUART0_RX/FB_CS5_b/FB_TSIZ1/FB_BE23_16_BLS15_8_b
PTC17/LPUART0_TX/FB_CS4_b/FB_TSIZ0/FB_BE31_24_BLS7_0_b
PTC18/LPUART0_RTS_b/FB_TBST_b/FB_CS2_b/FB_BE15_8_BLS23_16_b
PTC19/LPUART0_CTS_b/FB_CS3_b/FB_BE7_0_BLS31_24_b/FB_TA_b
B9
D8
C8
B8
A8
D7
C7
B7
A7
D6
C6
C5
B6
A6
A5
B5
D5
C4
B4
A4
R27046 DEBUG_SL 2K 0402
R27047 DEBUG_SL 2K 0402
PMIC_EN_R [29]
KIP_IO [29,31,48]
PLT_RST_BUF_N [22,34,38,43,44,56]
SL_PG [56,69]
DEBUG_MUX_S3 [31]
GP_SAM_COLD_BOOT [56]
RTCRST_CTRL_R [29]
SAM_PCH_RSMRST_N_R [29]
VCCRTC_RST [56]
DEBUG_MUX_S2 [31]
I2C_ROP_SCL [31,63,70]
I2C_ROP_SDA [31,63,70]
SB_PWRBTN_SR [29]
SAM_PCH_INT1 [25]
SL_UART_SEL_N [69]
BRDID_ADC_RD_EN [28,29]
SAM_THERM1 [39]
SL_ADC_RD_EN [69]
SL_3P3V_DIS [46]
SSD_FLUSH_DONE [43,56]
MK22FN512VDC12
PU Resistors are on PCH side
SKL_RTCRST_N [20]
Q27001
RUM002N02GT2L
G
D
S
[29] RTCRST_CTRL
R27005
100K
0201
Title: 27. SAM_1, K22
Microsoft Confidential
Engineer:
Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
Sheet 27 of 79



Title:	28. SAM_2, K22		
Microsoft Confidential	Engineer:	Surface	
Size: C	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 28 of 79		


3P3VA_SW
R29061
200K
0201
U27001D
PORT - D
PTD0/LLWU_P12/SPI0_PCS0/UART2_RTS_b/FTM3_CH0/FB_ALE/FB_CS1_b/FB_TS_b/LPUART0_RTS_b
PTD1/ADC0_SE5b/SPI0_SCK/UART2_CTS_b/FTM3_CH1/FB_CS0_b/LPUART0_CTS_b
PTD2/LLWU_P13/SPI0_SOUT/UART2_RX/FTM3_CH2/FB_AD4/I2C0_SCL/LPUART0_RX
PTD3/SPI0_SIN/UART2_TX/FTM3_CH3/FB_AD3/I2C0_SDA/LPUART0_TX
PTD4/LLWU_P14/SPI0_PCS1/UART0_RTS_b/FTM0_CH4/FB_AD2/EWM_IN/SPI1_PCS0
PTD5/ADC0_SE6b/SPI0_PCS2/UART0_CTS_b/FTM0_CH5/FB_AD1/EWM_OUT_b/SPI1_SCK
PTD6/ADC0_SE7b/LLWU_P15/SPI0_PCS3/UART0_RX/FTM0_CH6/FB_AD0/FTM0_FLT0/SPI1_SOUT
PTD7/UART0_TX/FTM0_CH7/FTM0_FLT1/SPI1_SIN
PTD8/I2C0_SCL/LPUART0_RX/FB_A16
PTD9/I2C0_SDA/LPUART0_TX/FB_A17
PTD10/LPUART0_RTS_b/FB_A18
PTD11/LPUART0_CTS_b/FB_A19
PTD12/FTM3_FLT0/FB_A20
PTD13/FB_A21
PTD14/FB_A22
PTD15/FB_A23
D4
D3
C3
B3
A3
A2
B2
A1
A10
A9
B1
C2
C1
D2
D1
E1
R29045 DEBUG_SL 2K 0402
R29019 100 0201
R29020 100 0201
499 R29076 0201
PSAM_SL_DBG_EN [29]
SAM_CHG_ACOK [63]
SL_UART_RX [69]
SL_UART_TX [69]
DEBUG_MUX_S0 [31]
SAM_CHGR_PSU_ON_R [29]
SAM_PWR_BTN_STATE [34,56]
SAM_SEN_HALL_INT [41]
I2C_SCL_MCU [34,39,59]
I2C_SDA_MCU [34,39,59]
BL_INST_ON_HNDSHK [10,30]
KIP_IO [27,31,48]
GP_DBGACC [31,47,56]
SPI1_EXT [37]
SAM_PROCHOT_R [29]
SAM_PCH_INT0 [25]
PORT - E
PTE5/SPI1_PCS2/LPUART0_RX/FTM3_CH0
PTE6/SPI1_PCS3/LPUART0_CTS_b/I2S0_MCLK/FTM3_CH1/USB_SOF_OUT
PTE24/ADC0_SE17/I2C0_SCL/EWM_OUT_b
PTE25/ADC0_SE18/I2C0_SDA/EWM_IN
PTE26/CLKOUT32K/RTC_CLKOUT/USB_CLKIN
G4
F3
H5
J5
H6
R29046 DEBUG_SL 2K 0402
SAM_KIP_UART_RX [48]
DEBUG_MUX_S1 [31]
SAM_PWRBTN_N [56]
DEBUG_LED0 [27]
PMIC_SAM_ALL_SYS_PWRGD [22,34,59]
MK22FN512VDC12
3P3VA_SW
DEBUG_SL
C29021
0.1u 6.3V
0201
U29020
VCC
PR
D
CK
CLR
GND
Q
Q
NC7SZ74L8X
DEBUG_SL
1
2
3
4
5
6
7
8
DEBUG_SL
R29072
0201
0
[27,28] BRDID_ADC_RD_EN
DEBUG_SL
R29073
0201
100
[29] PSAM_SL_DBG_EN
DEBUG_SL
R29074
20K
0201
DEBUG_SL
C29022
0.1u 6.3V
0201
DEBUG_SL
R29075
20K
0201
DEBUG_SL
C29023
0.1u 6.3V
0201
SAM_SL_DBG_EN [47]
PMIC_EN [58,59]
3P3V_SSD_EN [65]
SAM_PCH_RSMRST_N [18,22,56]
RTCRST_CTRL [27]
SAM_PMIC_PWRBTN [59]
VRM_PWR_EN [22,66]
SAM_CHGR_PSU_ON [34,63]
SAM_PROCHOT [10]
[27] PMIC_EN_R
[27] 3P3V_SSD_EN_R
[27] SAM_PCH_RSMRST_N_R
[27] RTCRST_CTRL_R
[27] SB_PWRBTN_SR
[29] SAM_CHGR_PSU_ON_R
[29] SAM_PROCHOT_R
499 R29049 0201
499 R29050 0201
499 R29051 0201
499 R29052 0201
0 R29053 0201
499 R29055 0201
499 R29056 0201
MTP29001
MTP29002
MTP29003
MTP29004
MTP29005
MTP29006
MTP29007
MTP29008
Title: 29. SAM_3, K22
Microsoft Confidential
Engineer:
Surface
Size B
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
Sheet 29 of 79

When BL_INST_ON_HNDSHK is LOW, SAM controls BKLT.
When BL_INST_ON_HNDSHK is HIGH, SOC controls BKLT.

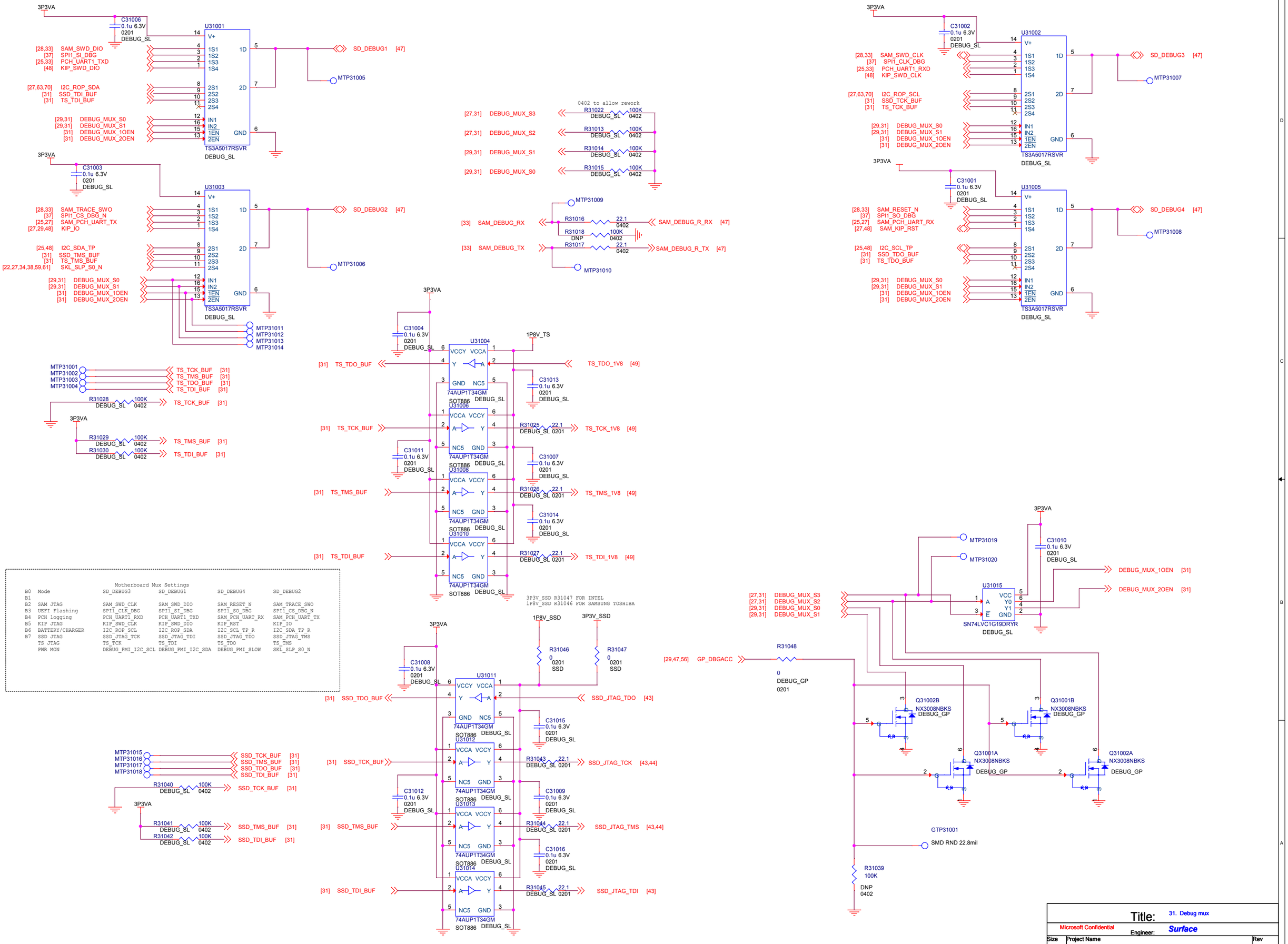


PANEL_LOGO [55]

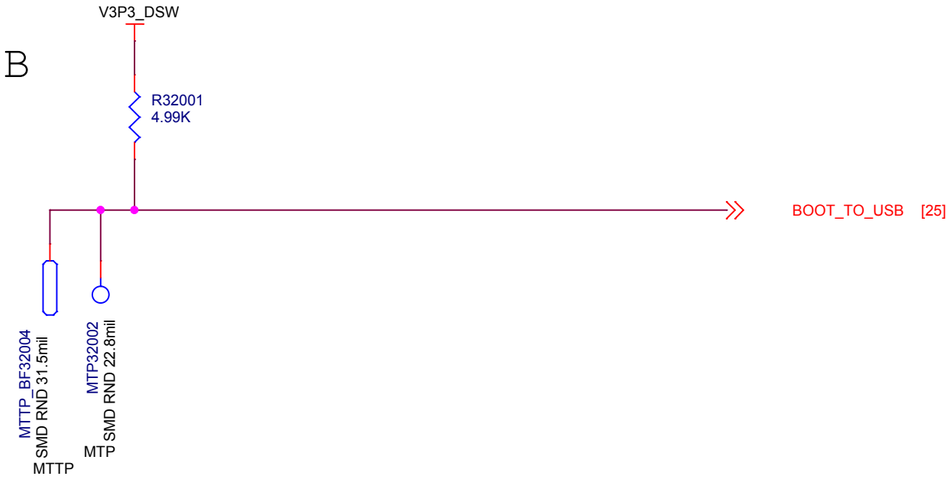
35kohms-287kohms pulldown at TDM
PANEL_LOGO Input is 3.3V tolerant

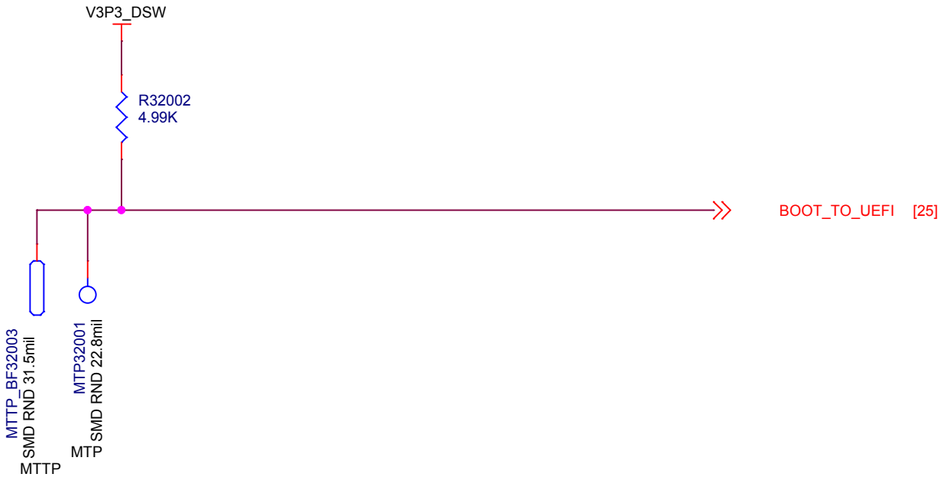
[27,30] SAM_PANEL_LOGO_EN — R30014 — 100 0201

Title:	30. INSTANT_ON	
Microsoft Confidential	Engineer:	Surface
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 30 of 79	

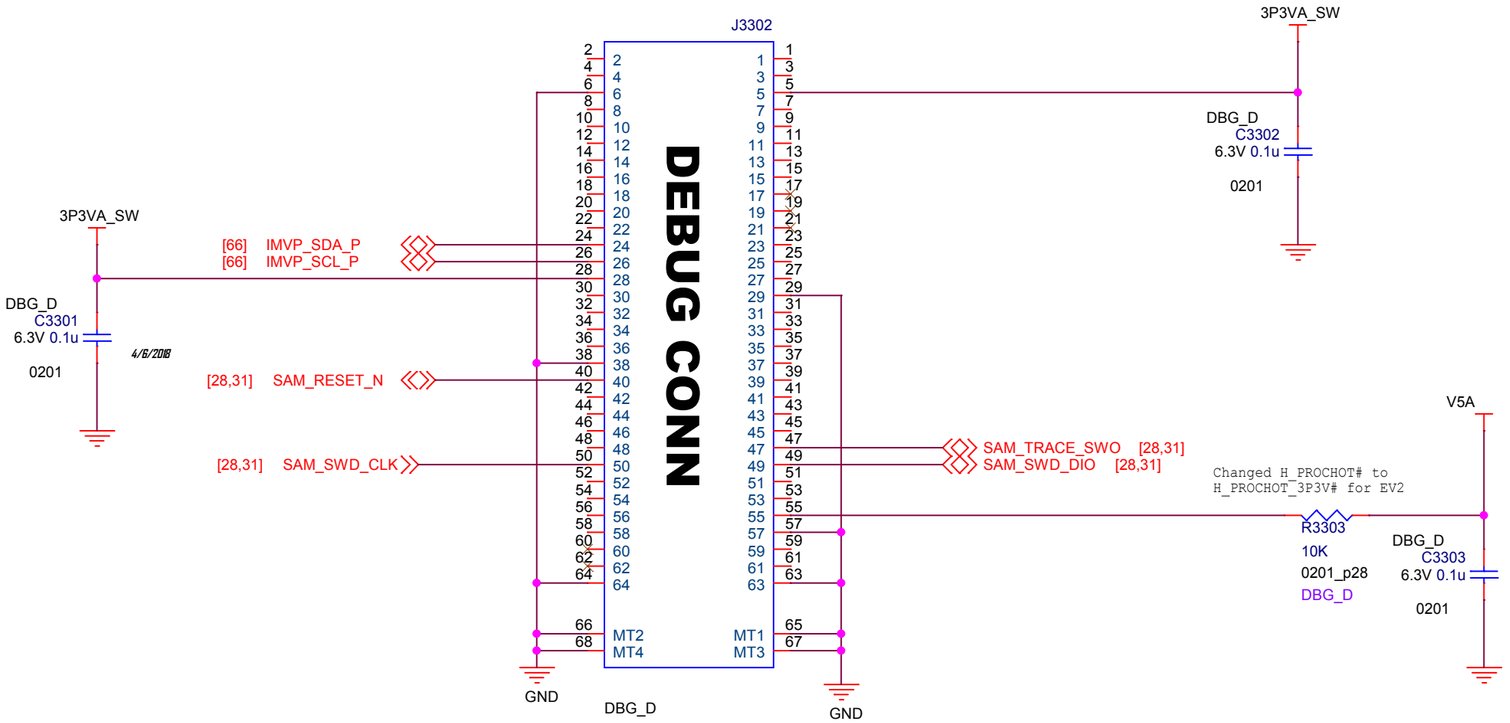

3P3VA
C31006
0.1u 6.3V
0201
DEBUG_SL
U31001
V+
1S1
1S2
1S3
1S4
2S1
2S2
2S3
2S4
IN1
IN2
1EN
2EN
1D
2D
GND
TS3A5017RSVR
DEBUG_SL
[28,33] SAM_SWD_DIO
[37] SPI1_SI_DBG
[25,33] PCH_UART1_TXD
[48] KIP_SWD_DIO
[27,63,70] I2C_ROP_SDA
[31] SSD_TDI_BUF
[31] TS_TDI_BUF
[29,31] DEBUG_MUX_S0
[29,31] DEBUG_MUX_S1
[31] DEBUG_MUX_1OEN
[31] DEBUG_MUX_2OEN
SD_DEBUG1 [47]
MTP31005
C31003
U31003
[28,33] SAM_TRACE_SWO
[37] SPI1_CS_DBG_N
[25,27] SAM_PCH_UART_TX
[27,29,48] KIP_IO
[25,48] I2C_SDA_TP
[31] SSD_TMS_BUF
[31] TS_TMS_BUF
[22,27,34,38,59,61] SKL_SLP_S0_N
SD_DEBUG2 [47]
MTP31006
MTP31011
MTP31012
MTP31013
MTP31014
MTP31001
MTP31002
MTP31003
MTP31004
TS_TCK_BUF [31]
TS_TMS_BUF [31]
TS_TDO_BUF [31]
TS_TDI_BUF [31]
R31028 100K DEBUG_SL 0402 TS_TCK_BUF [31]
R31029 100K DEBUG_SL 0402 TS_TMS_BUF [31]
R31030 100K DEBUG_SL 0402 TS_TDI_BUF [31]
0402 to allow rework
[27,31] DEBUG_MUX_S3
[27,31] DEBUG_MUX_S2
[29,31] DEBUG_MUX_S1
[29,31] DEBUG_MUX_S0
R31022 100K DEBUG_SL 0402
R31013 100K DEBUG_SL 0402
R31014 100K DEBUG_SL 0402
R31015 100K DEBUG_SL 0402
MTP31009
[33] SAM_DEBUG_RX
R31016 22.1 0402
SAM_DEBUG_R_RX [47]
R31018 DNP 100K 0402
[33] SAM_DEBUG_TX
R31017 22.1 0402
SAM_DEBUG_R_TX [47]
MTP31010
C31004
U31004
VCCY VCCA
Y A
GND NC5
74AUP1T34GM
SOT886 DEBUG_SL
1P8V_TS
[31] TS_TDO_BUF
TS_TDO_1V8 [49]
C31013
0.1u 6.3V
0201
DEBUG_SL
U31006
VCCA VCCY
A Y
NC5 GND
[31] TS_TCK_BUF
R31025 22.1 DEBUG_SL 0201 TS_TCK_1V8 [49]
C31011
U31008
[31] TS_TMS_BUF
R31026 22.1 DEBUG_SL 0201 TS_TMS_1V8 [49]
C31007
C31014
U31010
[31] TS_TDI_BUF
R31027 22.1 DEBUG_SL 0201 TS_TDI_1V8 [49]
3P3V_SSD R31047 FOR INTEL
1P8V_SSD R31046 FOR SAMSUNG TOSHIBA
1P8V_SSD
3P3V_SSD
R31046 0 0201 SSD
R31047 0 0201 SSD
C31008
U31011
[31] SSD_TDO_BUF
SSD_JTAG_TDO [43]
C31015
MTP31015
MTP31016
MTP31017
MTP31018
SSD_TCK_BUF [31]
SSD_TMS_BUF [31]
SSD_TDO_BUF [31]
SSD_TDI_BUF [31]
R31040 100K DEBUG_SL 0402 SSD_TCK_BUF [31]
R31041 100K DEBUG_SL 0402 SSD_TMS_BUF [31]
R31042 100K DEBUG_SL 0402 SSD_TDI_BUF [31]
C31012
U31012
[31] SSD_TCK_BUF
R31043 22.1 DEBUG_SL 0201 SSD_JTAG_TCK [43,44]
C31009
U31013
[31] SSD_TMS_BUF
R31044 22.1 DEBUG_SL 0201 SSD_JTAG_TMS [43,44]
C31016
U31014
[31] SSD_TDI_BUF
R31045 22.1 DEBUG_SL 0201 SSD_JTAG_TDI [43]
Motherboard Mux Settings
B0 Mode | SD_DEBUG3 | SD_DEBUG1 | SD_DEBUG4 | SD_DEBUG2
B1
B2 SAM JTAG | SAM_SWD_CLK | SAM_SWD_DIO | SAM_RESET_N | SAM_TRACE_SWO
B3 UEFI Flashing | SPI1_CLK_DBG | SPI1_SI_DBG | SPI1_SO_DBG | SPI1_CS_DBG_N
B4 PCH logging | PCH_UART1_RXD | PCH_UART1_TXD | SAM_PCH_UART_RX | SAM_PCH_UART_TX
B5 KIP JTAG | KIP_SWD_CLK | KIP_SWD_DIO | KIP_RST | KIP_IO
B6 BATTERY/CHARGER | I2C_ROP_SCL | I2C_ROP_SDA | I2C_SCL_TP_R | I2C_SDA_TP_R
B7 SSD JTAG | SSD_JTAG_TCK | SSD_JTAG_TDI | SSD_JTAG_TDO | SSD_JTAG_TMS
TS JTAG | TS_TCK | TS_TDI | TS_TDO | TS_TMS
PWR MON | DEBUG_PMI_I2C_SCL | DEBUG_PMI_I2C_SDA | DEBUG_PMI_SLOW | SKL_SLP_S0_N
C31002
U31002
[28,33] SAM_SWD_CLK
[37] SPI1_CLK_DBG
[25,33] PCH_UART1_RXD
[48] KIP_SWD_CLK
[27,63,70] I2C_ROP_SCL
[31] SSD_TCK_BUF
[31] TS_TCK_BUF
SD_DEBUG3 [47]
MTP31007
C31001
U31005
[28,33] SAM_RESET_N
[37] SPI1_SO_DBG
[25,27] SAM_PCH_UART_RX
[27,48] SAM_KIP_RST
[25,48] I2C_SCL_TP
[31] SSD_TDO_BUF
[31] TS_TDO_BUF
SD_DEBUG4 [47]
MTP31008
MTP31019
MTP31020
C31010
U31015
VCC
A Y0
Y1
E GND
SN74LVC1G19DRYR
DEBUG_SL
DEBUG_MUX_1OEN [31]
DEBUG_MUX_2OEN [31]
[27,31] DEBUG_MUX_S3
[27,31] DEBUG_MUX_S2
[29,31] DEBUG_MUX_S0
[29,31] DEBUG_MUX_S1
R31048
[29,47,56] GP_DBGACC
0
DEBUG_GP
0201
Q31002B
NX3008NBKS
DEBUG_GP
Q31001B
Q31001A
Q31002A
GTP31001
SMD RND 22.8mil
R31039
100K
DNP
0402
Title: 31. Debug mux
Microsoft Confidential
Engineer: Surface
Size C
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
Sheet 31 of 79

BOOT_TO_USB





Title:	32. Debug Buttons		
Microsoft Confidential	Engineer:	*Surface*	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 32 of 79		



DVi7U7660s16s512x2Retail

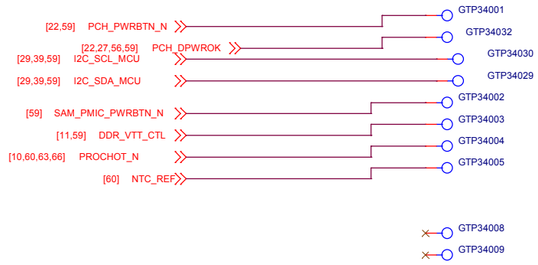
Title: 33. SW Debug Conn

Microsoft Confidential

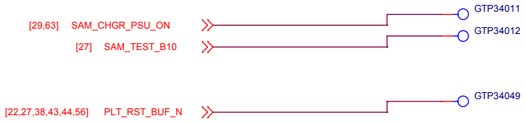
Engineer: Surface

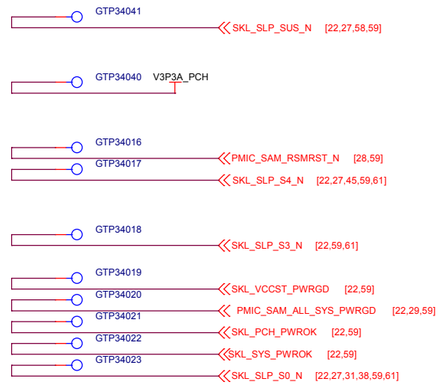
Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 33 of 79



I2C testpoints are shown on page 25





DVI7U7660s16s512x2Retail

Title: 34. EE Debug Connector		
Size: A2	Document Number: A	Rev: <RevCode>
Date: Thursday, April 26, 2018	Sheet 34 of 76	

Title: 35. EMPTY

Microsoft Confidential

Engineer: *Surface*

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 35 of 79

MTP36003
SMD RND 22.8mil

SMD RND 22.8mil
MTP36001

MTP36002
SMD RND 22.8mil

No Power Monitors in this SKU

Resistor Address for MAX3440
20.5K => 0x3C/0x3D
11.0K => 0x38/0x39
5.90K => 0x34/0x35
3.16K => 0x30/0x31
1.74K => 0x2C/0x2D
931K => 2x28/2x29
499 => 2x24/2x25
GND => 2x20/2x21

Title: 36. Power Monitor

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
Custom	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 36 of 79

UEFI SPI ROM

3VSUS_ORG

1K
0201
R37001

(128Mb=16MB @104MHz)

Needs to >= 66MHz

U37001
W25Q128JVPIQ

SPI1_CS0_N	1	CS#	VCC	8	
SPI1_SO	2	DO(IO1)	HOLD#(IO3)	7	SPI1_HOLD_N
SPI1_WP_N	3	WP#(IO2)	CLK	6	SPI1_CLK
	4	GND1	DI(IO0)	5	SPI1_SI
	9	GND2			

3VSUS_ORG

C37001
0.1u 6.3V
0201

3VSUS_ORG

C37002
0.1u 6.3V
0201
DEBUG_SL

DEBUG_SL
U37002
TS3A27518EZQSR

SPI1_CLK	A1	COM1	V+	C2	
SPI1_SI	B1	COM2			
SPI1_SO	C1	COM3	EN#	C4	
SPI1_WP_N	D1	COM4			
SPI1_HOLD_N	E1	COM5	IN1	B4	
SPI1_CS0_N	D2	COM6	IN2	D3	
			GND	C3	
	A3	N.C.			
[21] SPI_CLK	B3	NC1	NO1	E2	SPI1_CLK_DBG [31]
[21] SPI_SI	A2	NC2	NO2	E3	SPI1_SI_DBG [31]
[21] SPI_SO	A4	NC3	NO3	E4	SPI1_SO_DBG [31]
[21] SPI_WP_IO2	B5	NC4	NO4	D5	SPI1_WP_DBG_N
[21] SPI_HOLD_IO3_N	C5	NC5	NO5	D4	SPI1_HOLD_DBG_N
[21] SPI_CS0_N	A5	NC6	NO6	E5	SPI1_CS_DBG_N [31]

BGA24

DEBUG_SL
R37005 100K 0201

MTTP37001
SMD RND 22.8mil

3VSUS_ORG

1K
0201
DEBUG_SL
R37003

1K
0201
DEBUG_SL
R37004

SPI1_EXT [29]

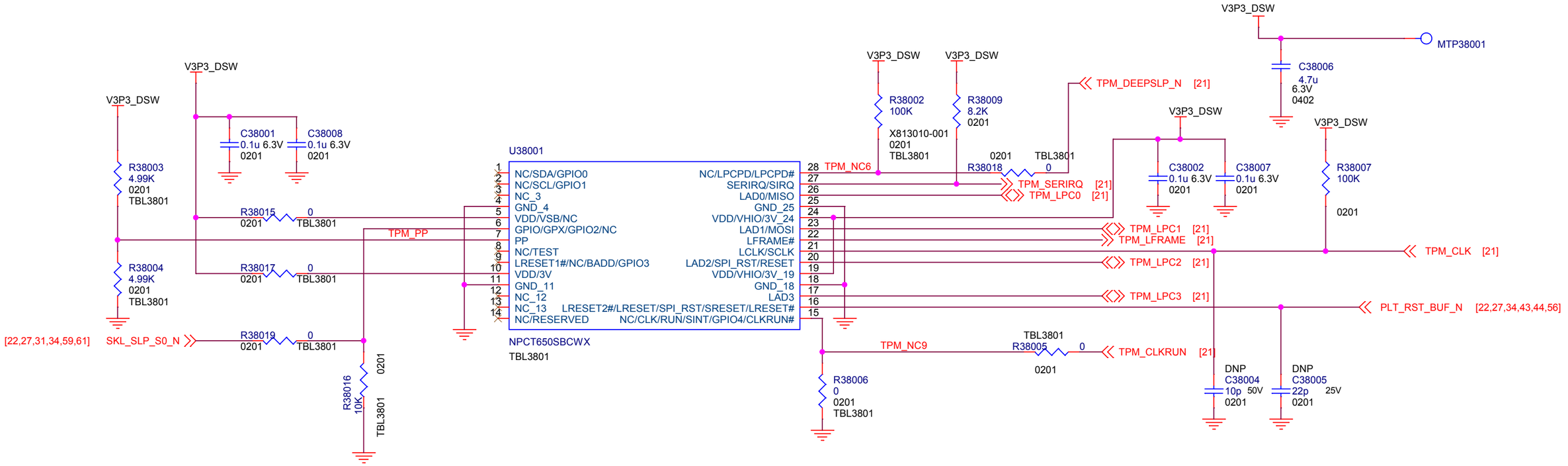
SPI_CLK = 20/33/50Mhz

SPI1_CLK	R37006	0	NDEBUG_SL	0201	SPI_CLK	MTTP37002 SMD RND 22.8mil
SPI1_SI	R37007	0	NDEBUG_SL	0201	SPI_SI	MTTP37003 SMD RND 22.8mil
SPI1_SO	R37008	0	NDEBUG_SL	0201	SPI_SO	MTTP37004 SMD RND 22.8mil
SPI1_WP_N	R37009	0	NDEBUG_SL	0201	SPI_WP_IO2	MTTP37005 SMD RND 22.8mil
SPI1_HOLD_N	R37010	0	NDEBUG_SL	0201	SPI_HOLD_IO3_N	MTTP37006 SMD RND 22.8mil
SPI1_CS0_N	R37011	0	NDEBUG_SL	0201	SPI_CS0_N	MTTP37007 SMD RND 22.8mil

```
IN1/IN2 = L  => COM to NC
IN1/IN2 = H  => NC  to COM
```

Title: 37. SPI ROM UEFI			
Microsoft Confidential	Engineer: Surface		
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Tuesday, May 01, 2018	Sheet 37 of 79		

Trusted Platform Module



TBL3801		
Lancelot RefDes	***Nuvuton***	***NationZ***
U38001	M1006791-002	X930840-002
R38002	NO STUFF	X813010-001
R38003	NO STUFF	NO STUFF
R38004	X813007-001	NO STUFF
R38005	X811786-001	NO STUFF
R38006	NO STUFF	X811786-001
R38015	X811786-001	NO STUFF
R38016	NO STUFF	NO STUFF
R38017	X811786-001	X811786-001
R38018	X811786-001	NO STUFF
R38019	X811786-001	NO STUFF

Title: 38. TPM

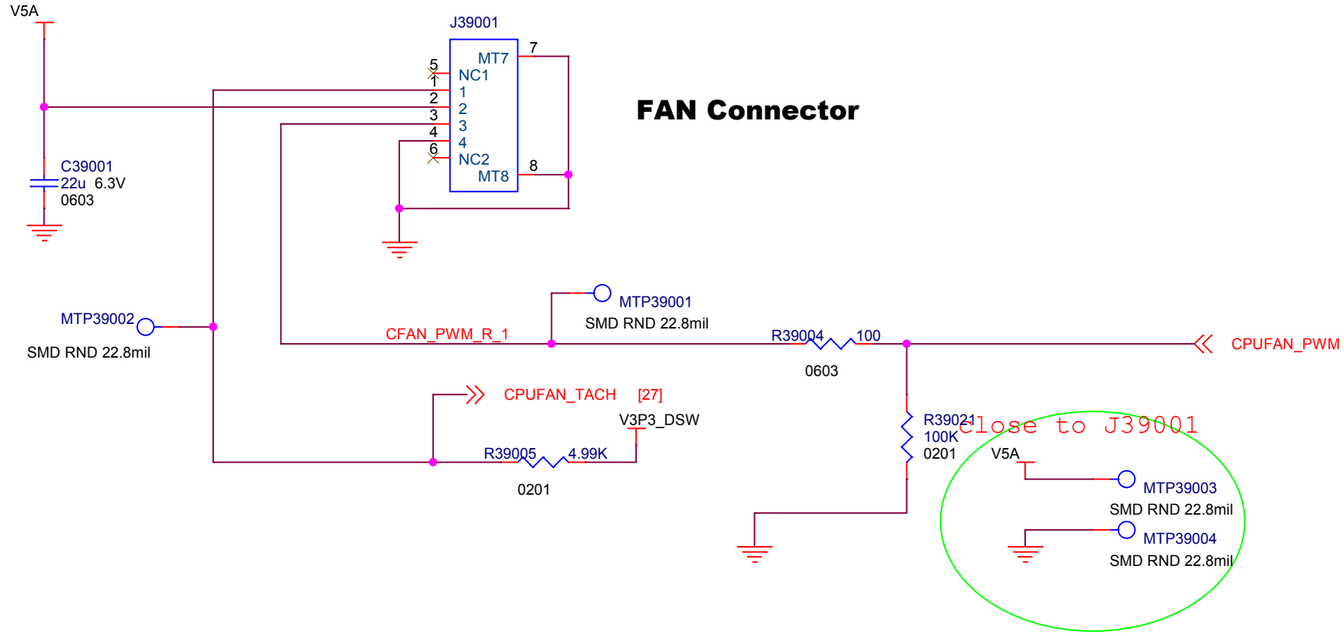
Microsoft Confidential

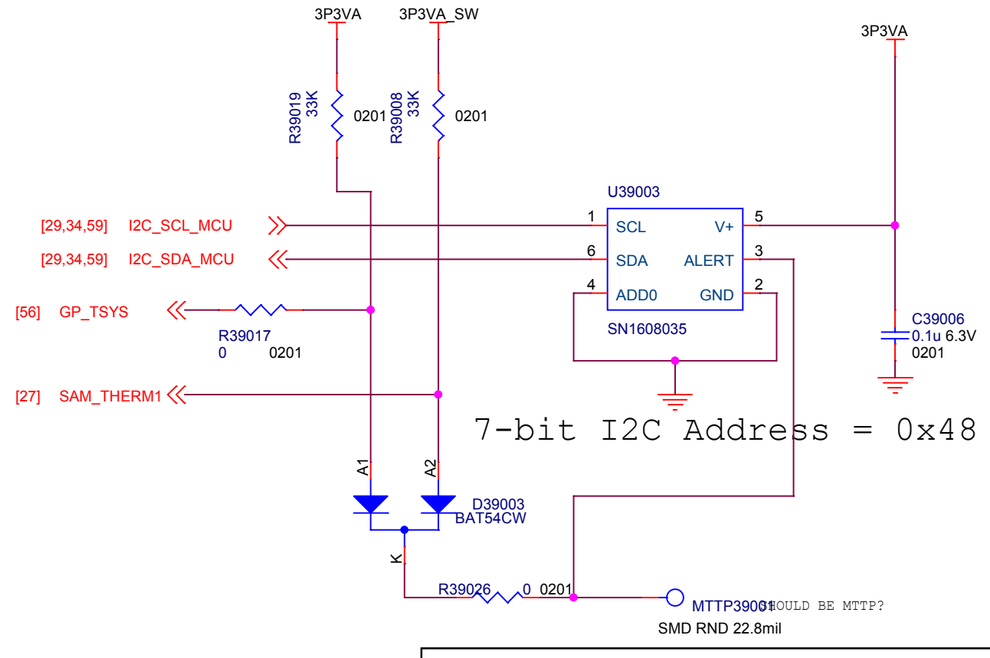
Engineer: *Surface*

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 38 of 79

FAN Connector





U SPECIFIC

Title:	39. Temp Sensor/System Fan	
Microsoft Confidential	Engineer: Surface	
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Tuesday, May 01, 2018	Sheet 39 of 79	

SPKR Trace Width
1. Maximum trace resistance for each channel less than 0.5 ohms.
2. Each of 4 traces, measured from CODEC to speaker connector, less than 0.25 ohms

C40009 and C40010 can be deleted and L40001 converted to a 0 ohm jumper if smart amp remains.

Place close to J41001

Place under U40001

close to audio

ALC3269C-GRT

Microsoft Confidential

Title: 40. REALTEK ALC3269 CODEC

Engineer: Surface

Size	Project Name	Rev
A3	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 40 of 79

Audio Jack/MIC1 Combo Jack

V3P3_DSW
SMD RND 22.8mil
MTP41011
R41015
499K
0201
SAM_SEN_HALL_INT [29]
C41016
6.3V
0.1u
J41005
PINS MIRRORED
MTG2 MTG1
MTG4 MTG3
502426-0810

R41001
[40] MIC1_VREFO_L
2.2K 0201

L41001 place close to J41004

C41001
4.7uF
6.3V
0402
R41002
1K
0201
L41001
120 OHM,100MHZ
0603
BLM18SG121TN1D
[40] MIC1_R
C41015
4.7uF
6.3V
0402
[40] MIC1_L
R41003
22K
0201
C41002
25V 100p
0201
AGND
AGND

PCB trace width of MIC1-R/Mic1-L (Sleeve/Ring2) are required at least 40 mil for HP crosstalk consideration and its length should be as short as possible

MIC1_R_CR_F_C
[40] COMBO_JACK
R41004 22K
0201
C41004
10u 6.3V
0402
AGND

SMD RND 22.8mil
MTP41001
HPOUT_JD [40]
D41001
V5.5MLA0402NR
CDS2C05GTA
A2
A1
GND

[40] HPOUT_L
[40] HPOUT_R
R41005 51.1 0603
R41006 51.1 0603
HPOUT_L_F
HPOUT_R_F
L41002 BLM18SG121TN1D 120 OHM,100MHZ 0603
L41003 BLM18SG121TN1D 120 OHM,100MHZ 0603
R41007 10K 0201
R41008 10K 0201
C41005 100p 25V 0201
C41006 100p 25V 0201
AGND
AGND
GND
GND
D41002 V5.5MLA0402NR
D41003 V5.5MLA0402NR
HPOUT_L_F_C
HPOUT_R_F_C
MTP41004 SMD RND 22.8mil
MTP41005 SMD RND 22.8mil
MTP41002 SMD RND 22.8mil
DNP
J41004
MIC1_R_CR_F_C
1 MIC
3 RIGHT
4 DET
5 LEFT
2 GND
AGND
MTP41003 SMD RND 22.8mil
D41004 V5.5MLA0402NR
GND

SPKR

[42] AMP_SPK_RP
[42] AMP_SPK_RN
C41007 1000p 25V 0201
C41008 25V 1000p 0201
GND
SMD RND 22.8mil MTP41006
MTP41007 SMD RND 22.8mil
D41005 V14MLA0603NH
D41006 V14MLA0603NH
J41002 78171-0002 X872411-001
1 2 3 4
MTG1 MTG2
GND
GND

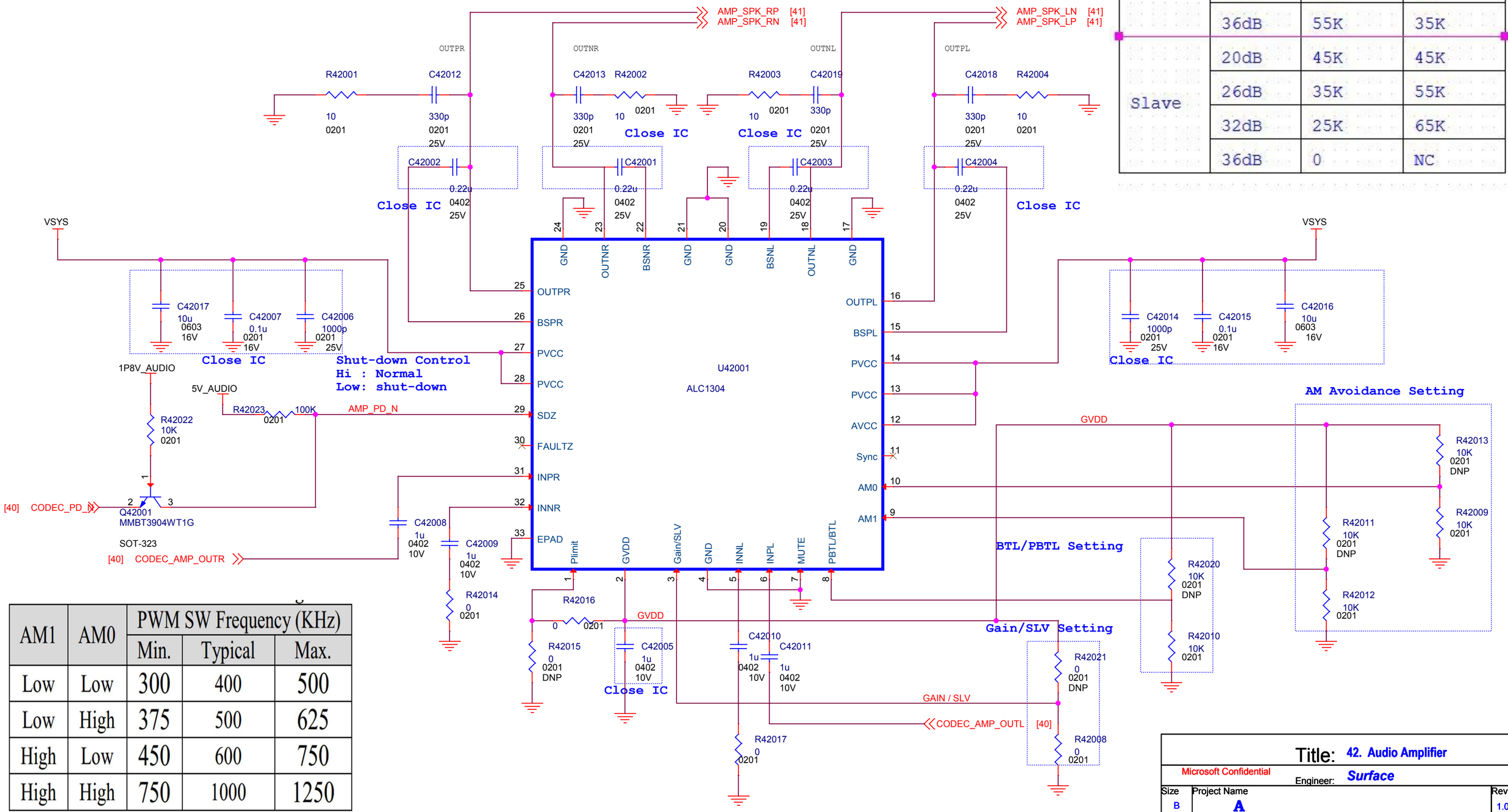
[42] AMP_SPK_LP
[42] AMP_SPK_LN
C41009 1000p 25V 0201
C41010 25V 1000p 0201
GND
SMD RND 22.8mil MTP41008
MTP41009 SMD RND 22.8mil
D41007 V14MLA0603NH
D41008 V14MLA0603NH
J41003 78171-0002 X872411-001
1 2 3 4
MTG1 MTG2
GND
GND

Title: 41. Audio Jack/Spkr
Microsoft Confidential
Engineer: Surface
Size C | Project Name A | Rev 1.0.0.1
Date: Thursday, April 26, 2018 | Sheet 41 of 79

Stereo Input(S.E.)
Stereo Output-BTL

SPKR Trace Width
1. Maximum trace resistance for each channel less than 0.5 ohms.
2. Each of 4 traces, measured from CODEC to speaker connector, less than 0.25 ohms

Mode	Gain	RX(ohm)	RY(ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	36dB	55K	35K
Slave	20dB	45K	45K
	26dB	35K	55K
	32dB	25K	65K
	36dB	0	NC



AM1	AM0	PWM SW Frequency (KHz)		
		Min.	Typical	Max.
Low	Low	300	400	500
Low	High	375	500	625
High	Low	450	600	750
High	High	750	1000	1250

Microsoft Confidential

Title: 42. Audio Amplifier

Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 42 of 79

For common BGA SSDs

U43001A

[20] PCIECLK_SSD_DP — R43011 0 0402 — D4 REFCLK_P
[20] PCIECLK_SSD_DN — R43012 0 0402 — D5 REFCLK_N

[24] PCIE_SSD_TX7_DP — F4 SATAmAp/PERp0
[24] PCIE_SSD_TX7_DN — F5 SATAmAm/PERn0

[24] PCIE_SSD_RX7_DP — SSD 0.22u 0201 6.3V SSD — H4 SATAmBp/PETp0
[24] PCIE_SSD_RX7_DN — 0.22u 0201 6.3V C43001 — H5 SATAmBm/PETn0
C43002

[24] PCIE_SSD_TX8_DP — K4 PER_P1
[24] PCIE_SSD_TX8_DN — K5 PER_N1

[24] PCIE_SSD_RX8_DP — SSD 0.22u 0201 6.3V SSD — M4 PET_P1
[24] PCIE_SSD_RX8_DN — 0.22u 0201 6.3V C43004 — M5 PET_N1
C43005

P4 PERp2/NC_P4
P5 PERn2/NC_P5

1P8V_SSD
0201 C43003 0.1u 6.3V SSD GND
SSD_PERST_N [44] — T4 PETp2/NC_T4
T5 PETn2/NC_T5

V4 PERp3/NC_V4
V5 PERn3/NC_V5

SMD RND 22.8mil MTP43024
Y4 PETp3/NC_Y4
Y5 PETn3/NC_Y5

[22,27,34,38,44,56] PLT_RST_BUF_N
[25,44] PCIE_SSD_PERST_N
U43002 SSD SN74AUP1G08DRYR
D7 PERST#

GND
SSD R43003 100K 1% 0201 GND
F14 PEDET

D8 CLKREQ#

D14 SUSCLK/NC_D14

[20] SSD_PCIECLK_REQ_N — E8 DEVSLP/NC_E8

E12 PEWAKE#/NC_E12

GTP43003 SMD RND 22.8mil — W7 LED1# /DAS

R43098 1M DNP 0402 XRCGB25M000F2P00R0
0201 C43099 DNP 10p 25V
Y43001 1 3 2 4 DNP
C43098 10p 0201 25V DNP
SSD_XTAL_OUT — B6 CAL_P/NC_B6
SSD_XTAL_IN — C7 XTAL_ OUT/NC_C7
C8 XTAL_IN/NC_C8

C10 RZQ_1/NC_C10

[43] SSD_DIAG1 — SSD_DIAG1 — D13 DIAG1/I2C_DATA
[43,44] SSD_DIAG0 — SSD_DIAG0 — E13 DIAG0/I2C_CLK

L18 JTAG_TRST#/NC_L18

[31,43,44] SSD_JTAG_TCK — N17 JTAG_TCK
[31,43,44] SSD_JTAG_TMS — N18 JTAG_TMS
[31,43] SSD_JTAG_TDI — R17 JTAG_TDI
[43,44] SSD1_JTAG_TDO — R18 JTAG_TDO

U17 SMB_ CLK/NC_U17
U18 SMB_DATA/NC_U18
W18 ALERT#/NC_W18
AA10 RZQ_2/NC_AA10

GTP43014 SMD RND 22.8mil
GTP43013 SMD RND 22.8mil

HFB1M8MO331A0MR

U43001C

C1 GND_C1 — GND_M10 M10
C2 GND_C2 — GND_N1 N1
C3 GND_C3 — GND_N2 N2
C4 GND_C4 — GND_N3 N3
C5 GND_C5 — GND_N4 N4
C15 GND_C15 — GND_N5 N5
D6 GND_D6 — GND_N14 N14
D11 GND_D11 — GND_N15 N15
E1 GND_E1 — GND_P7 P7
E2 GND_E2 — GND_P8 P8
E3 GND_E3 — GND_P9 P9
E4 GND_E4 — GND_P10 P10
E5 GND_E5 — GND_P11 P11
E6 GND_E6 — GND_P12 P12
E7 GND_E7 — GND_R1 R1
E11 GND_E11 — GND_R2 R2
E14 GND_E14 — GND_R3 R3
E15 GND_E15 — GND_R4 R4
F6 GND_F6 — GND_R5 R5
G1 GND_G1 — GND_R9 R9
G2 GND_G2 — GND_R10 R10
G3 GND_G3 — GND_R14 R14
G4 GND_G4 — GND_R15 R15
G5 GND_G5 — GND_T9 T9
G9 GND_G9 — GND_T10 T10
G10 GND_G10 — GND_U1 U1
G14 GND_G14 — GND_U2 U2
G15 GND_G15 — GND_U3 U3
H9 GND_H9 — GND_U4 U4
H10 GND_H10 — GND_U5 U5
J1 GND_J1 — GND_U9 U9
J2 GND_J2 — GND_U10 U10
J3 GND_J3 — GND_U14 U14
J4 GND_J4 — GND_U15 U15
J5 GND_J5 — GND_W1 W1
J9 GND_J9 — GND_W2 W2
J10 GND_J10 — GND_W3 W3
J14 GND_J14 — GND_W4 W4
J15 GND_J15 — GND_W5 W5
K7 GND_K7 — GND_W6 W6
K8 GND_K8 — GND_W11 W11
K9 GND_K9 — GND_W14 W14
K10 GND_K10 — GND_W15 W15
K11 GND_K11 — GND_Y6 Y6
K12 GND_K12 — GND_Y11 Y11
L1 GND_L1 — GND_Y13 Y13
L2 GND_L2 — GND_AA1 AA1
L3 GND_L3 — GND_AA2 AA2
L4 GND_L4 — GND_AA3 AA3
L5 GND_L5 — GND_AA4 AA4
L14 GND_L14 — GND_AA5 AA5
L15 GND_L15 — GND_AA14 AA14
M9 GND_M9 — GND_AA15 AA15

HFB1M8MO331A0MR

U43001D

DNU_A1 A1
DNU_A2 A2
DNU_A4 A4
DNU_A6 A6
DNU_A8 A8 — SMD RND 22.8mil GTP43028
DNU_A11 A11
DNU_A13 A13
DNU_A15 A15
DNU_A17 A17
DNU_A18 A18
DNU_B1 B1
DNU_B2 B2
DNU_B4 B4
DNU_B8 B8 — SMD RND 22.8mil GTP43020
DNU_B11 B11
DNU_B13 B13
DNU_B15 B15
DNU_B17 B17
DNU_B18 B18
DNU_C6 C6
DNU_C9 C9
DNU_C11 C11
DNU_C12 C12
DNU_C16 C16
DNU/DDR_VDDQ C17 — SMD RND 22.8mil GTP43021
DNU_C17 C18 — SMD RND 22.8mil GTP43022
DNU_C18 D12
DNU_D12 E16
DNU_E16 E17
DNU_E17 E18
DNU_E18 G16
DNU_G16 G17
DNU_G17 G18
DNU_G18 J16
DNU_J16 J17
DNU_J17 J18
DNU_J18 L16
DNU_L16 L17
DNU/JTAG_TRST# N16
DNU_N16 R16
DNU_R16 U16
DNU_U16 W16
DNU_W16 W17
DNU_W17 Y7
C13 RFU_C13 — DNU/SSD_FLUSH Y8
C14 RFU_C14 — DNU/SSD_FLUSH_FB Y12
D15 RFU_D15 — DNU_Y12 Y14 — SMD RND 22.8mil GTP43029
F15 RFU_F15 — DNU_Y14 Y15
H14 RFU_H14 — DNU_Y15 AA6
H15 RFU_H15 — DNU_AA6 AA7
K14 RFU_K14 — DNU_AA7 AA8
K15 RFU_K15 — DNU_AA8 AA9
L7 RFU_L7 — DNU_AA9 AA11
L8 RFU_L8 — DNU_AA11 AA12
L9 RFU_L9 — DNU_AA12 AA13
L10 RFU_L10 — DNU_AA13 AA16
L11 RFU_L11 — DNU_AA16 AA17
L12 RFU_L12 — DNU/UART_RX AA18 — SMD RND 22.8mil GTP43024
M7 RFU_M7 — DNU/UART_TX AB1 — SMD RND 22.8mil GTP43025
M8 RFU_M8 — DNU_AB1 AB2
M11 RFU_M11 — DNU_AB2 AB4
M12 RFU_M12 — DNU_AB4 AB6
M14 RFU_M14 — DNU_AB6 AB8
M15 RFU_M15 — DNU_AB8 AB11
N7 RFU_N7 — DNU_AB11 AB13
N8 RFU_N8 — DNU_AB13 AB15
N9 RFU_N9 — DNU/VCCF AB17 — SMD RND 22.8mil GTP43027
N10 RFU_N10 — DNU_AB17 AB18
N11 RFU_N11 — DNU_AB18 AC1
N12 RFU_N12 — DNU_AC1 AC2
P14 RFU_P14 — DNU_AC2 AC4
P15 RFU_P15 — DNU_AC4 AC6
T14 RFU_T14 — DNU_AC6 AC8
T15 RFU_T15 — DNU_AC8 AC11
V14 RFU_V14 — DNU_AC11 AC13
V15 RFU_V15 — DNU_AC13 AC15
W8 RFU_W8 — DNU_AC15 AC17
W12 V_SEL0/RFU_W12 — DNU/VCCFQ AC18 — SMD RND 22.8mil GTP43026
W13 V_SEL1/RFU_W13 — DNU_AC18 — SMD RND 22.8mil GTP43023

HFB1M8MO331A0MR

C43101 4.7u 6.3V 0201 SSD

PCH_SSD_UART2_TXD [25]
PCH_SSD_UART2_RXD [25]

PCIE[12:1]_TXN/P : Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value, Gen3 = 176 to 265 nF; where 220 nF is nominal value
PCIE[12:1]_RXN/P : Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value, Gen3 = 176 to 265 nF; where 220 nF is nominal value

Difference between USB3 and PCIe: 1. No Choke, 2. Add cap on PER (p832 at DG v1.2)
RXN/RXP cap value must be different between Gen2 and Gen3
TX (from SOC) caps are at SOC side

Always ON logic, as like Intel RVP5.

GTP43012 SMD RND 22.8mil

1P2V_SSD

U43001B

G7 1p2v/1p1v/0p9v/RFU_G7
G8 1p2v/1p1v/0p9v/RFU_G8
G11 1p2v/1p1v/0p9v/RFU_G11
G12 1p2v/1p1v/0p9v/RFU_G12
H7 1p2v/1p1v/0p9v/RFU_H7
H8 1p2v/1p1v/0p9v/RFU_H8
H11 1p2v/1p1v/0p9v/RFU_H11
H12 1p2v/1p1v/0p9v/RFU_H12
J7 1p2v/1p1v/0p9v/RFU_J7
J8 1p2v/1p1v/0p9v/RFU_J8
J11 1p2v/1p1v/0p9v/RFU_J11
J12 1p2v/1p1v/0p9v/RFU_J12

1P8V_SSD

R7 V1P8_R7
R8 V1P8_R8
R11 V1P8_R11
R12 V1P8_R12
T7 V1P8_T7
T8 V1P8_T8
T11 V1P8_T11
T12 V1P8_T12
U7 V1P8_U7
U8 V1P8_U8
U11 V1P8_U11
U12 V1P8_U12

3P3V_SSD

D9 V3P3_D9
D10 V3P3_D10
E9 V3P3_E9
E10 V3P3_E10
W9 V3P3_W9
W10 V3P3_W10
Y9 V3P3_Y9
Y10 V3P3_Y10

HFB1M8MO331A0MR

V3P3_DSW

SMD RND 22.8mil GTP43015
R43018 100K 1% 0201 — 3P3V_SSD

U43006 TPS62085RLTR QFN-7
VIN 7, SW 6, EN 1, VOS 4, FB 3, GND 5, PG 2
C43034 10u 6.3V 0402
C43039 0.1u 6.3V 0201 GND
L43002 0.47uH X950133-001 2.5X2.0X1.2
R43025 82.5K 1% 0201 DNP
R43009 82.5K 1% 0201 SSD
C43041 100p 25V 0201 DNP
R43026 215K 1% 0201 DNP
R43010 165K 1% 0201 SSD
DNP C43035 22u 4V 20% 0603
C43036 22u 4V 20% 0603
C43037 22u 4V 20% 0603
C43038 22u 4V 20% 0603
SMD RND 22.8mil MTP43026
1P2V_SSD
R43150 10K 0201

R43010 is 215K for Samsung, 1P2V_SSD = 1.06V-1.15V + 100mV P-P ripple
R43010 is 165K for Toshiba, 1P2V_SSD = 1.2V +/- 5%
R43010 is 150K for Intel Pleasant Star, 1P2V_SSD = 1.24V+/- 4%
R43010 is 165K and R43009 is 24.9K for Hynix, 1P2V_SSD = 0.92V +/- 0.06V

R43023 0 0201 — 3P3V_SSD

SMD RND 22.8mil GTP43016
R43019 100K 1% 0201 — V3P3_DSW
R43134 100K 0201 GND

U43005 TPS62085RLTR QFN-7
VIN 7, SW 6, EN 1, VOS 4, FB 3, GND 5, PG 2
C43029 10u 6.3V 0402
C43080 0.1u 6.3V 0201 GND
L43001 0.47uH X950133-001 2.5X2.0X1.2
R43007 82.5K 1% 0201
C43040 100p 25V 0201 DNP
R43008 33K 1% 0201
R43024 33K 1% 0201
C43030 22u 4V 20% 0603
C43031 22u 4V 20% 0603
C43032 22u 4V 20% 0603
C43033 22u 4V 20% 0603
SMD RND 22.8mil MTP43027
1P8V_SSD

GTP43017 SMD RND 22.8mil — SSD_DIAG1 — SSD_DIAG1 [43]
GTP43018 SMD RND 22.8mil — SSD_DIAG0 — SSD_DIAG0 [43,44]

Load R43100 and DNP R43101 for U43001 loaded and U44007 DNP (Single SSD)
DNP R43100 and Load R43101 for both U43001 and U44007 loaded (Dual SSD)

[44] SSD2_JTAG_TDO
[43,44] SSD1_JTAG_TDO
R43100 0 0402 SSD
R43101 0 0402 SSD

SSD_JTAG_TDO [31] — MTP43020 SMD RND 22.8mil, MTP43021 SMD RND 22.8mil, MTP43022 SMD RND 22.8mil, MTP43023 SMD RND 22.8mil
[31,43,44] SSD_JTAG_TMS — SSD_JTAG_TMS
[31,43,44] SSD_JTAG_TCK — SSD_JTAG_TCK
[31,43] SSD_JTAG_TDI — SSD_JTAG_TDI
SSD_JTAG_TDO

3P3V_SSD
SSD C43006 6.3V 1u 0402
SSD C43007 6.3V 1u 0402
SSD C43008 0.1u 6.3V 0201
SSD C43009 0.1u 6.3V 0201
SSD C43010 6.3V 22u 0603
SSD C43011 6.3V 22u 0603

1P8V_SSD
SSD C43013 6.3V 1u 0402
SSD C43014 6.3V 1u 0402
SSD C43015 0.1u 6.3V 0201
SSD C43016 0.1u 6.3V 0201
SSD C43017 6.3V 22u 0603
SSD C43018 6.3V 22u 0603

1P2V_SSD
SSD C43019 6.3V 1u 0402
SSD C43020 6.3V 1u 0402
SSD C43021 0.1u 6.3V 0201
SSD C43022 0.1u 6.3V 0201
SSD C43023 0.1u 6.3V 0201
SSD C43024 0.1u 6.3V 0201
DNP C43025 6.3V 22u 0603
SSD C43026 6.3V 22u 0603

[56] GP_SSD_FLUSH — 499 R43113 0201 DNP
[27] SAM_SSD_FLUSH
MTP43025 SMD RND 22.8mil
R43108 200K 0201 DNP
R43109 200K 0201 DNP
U43007 74AUP1G32GX DNP
1P8V_SSD — DNP C43100 0.1u 6.3V 0201
R43120 4.7K 0201 DNP
R43123 4.7K 0201 DNP
SSD_DIAG0 [43,44]
GTP43019 SMD RND 22.8mil

1P8V_SSD2
1P8V_SSD
3P3V_SSD
R43124 100K 0201 DNP
R43121 100K 0201 DNP
R43125 4.7K 0201 DNP
R43122 4.7K 0201 DNP
Q43001A 2N7002KW DNP
3P3VA_SW
R43107 200K 0201
[43] SSD_DIAG1
SSD_FLUSH_DONE [27,56]
Q43001B 2N7002KW DNP
[44] SSD2_DIAG1
R43106 200K 0201 DNP
R43110 200K 0201 DNP

U SPECIFIC

Title:	43. SSD page 1		
Microsoft Confidential	Engineer:	Surface	
Size: A	Project Name: Custom		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 43 of 79		

For common BGA SSDs

U44007A

[20] PCIECLK_SSD2_DP — R44012 SSD 0 0402 — D4 REFCLK_P
[20] PCIECLK_SSD2_DN — R44013 SSD 0 0402 — D5 REFCLK_N

[24] PCIE_SSD2_TX11_DP — F4 SATAmAp/PERp0
[24] PCIE_SSD2_TX11_DN — F5 SATAmAm/PERn0

[24] PCIE_SSD2_RX11_DP — 0.22u 0201 6.3V SSD C44121 — H4 SATAmBp/PETp0
[24] PCIE_SSD2_RX11_DN — 0.22u 0201 6.3V SSD C44001 — H5 SATAmBm/PETn0

[24] PCIE_SSD2_TX12_DP — K4 PER_P1
[24] PCIE_SSD2_TX12_DN — K5 PER_N1

[24] PCIE_SSD2_RX12_DP — 0.22u 0201 6.3V SSD C44002 — M4 PET_P1
[24] PCIE_SSD2_RX12_DN — 0.22u 0201 6.3V SSD C44003 — M5 PET_N1

[43] SSD_PERST_N — P4 PERp2/NC_P4
P5 PERn2/NC_P5

T4 PETp2/NC_T4
T5 PETn2/NC_T5

V4 PERp3/NC_V4
V5 PERn3/NC_V5

Y4 PETp3/NC_Y4
Y5 PETn3/NC_Y5

1P8V_SSD
0201 C44118 0.1u 6.3V DNP GND

U44002 SN74AUP1G08DRYR
[22,27,34,38,43,56] PLT_RST_BUF_N
[25,43] PCIE_SSD_PERST_N
R44126 0 0201
DNP R44010 100K 0201 GND
D7 PERST#

F14 PEDET

D8 CLKREQ#

D14 SUSCLK/NC_D14

E8 DEVSLP/NC_E8

E12 PEWAKE#/NC_E12

[20] SSD2_PCIECLK_REQ_N
GTP44001 SMD RND 22.8mil
W7 LED1#/ DAS

DNP R44016 1M 0402
XRCGB25M000F2P00R0 Y44001
25V DNP C44120 10p 0201
DNP C44122 25V 10p 0201 DNP
SSD2_XTAL_OUT — B6 CAL_P/NC_B6
SSD2_XTAL_IN — C7 XTAL_OUT/NC_C7
C8 XTAL_IN/NC_C8

[43] SSD2_DIAG1 — SSD2_DIAG1 — C10 RZQ_1/NC_C10
D13 DIAG1/I2C_DATA

[43] SSD_DIAG0 — SSD_DIAG0 — E13 DIAG0/I2C_CLK

L18 JTAG_TRST#/NC_L18

[31,43] SSD_JTAG_TCK — SSD_JTAG_TCK — N17 JTAG_TCK
[31,43] SSD_JTAG_TMS — SSD_JTAG_TMS — N18 JTAG_TMS
[43] SSD1_JTAG_TDO — R17 JTAG_TDI
[43] SSD2_JTAG_TDO — SSD2_JTAG_TDO — R18 JTAG_TDO

U17 SMB_CLK/NC_U17
U18 SMB_DATA/NC_U18
W18 ALERT#/NC_W18
AA10 RZQ_2/NC_AA10

GTP44004 SMD RND 22.8mil
GTP44003 SMD RND 22.8mil

HFB1M8MO331A0MR

U44007C

C1	GND_C1	GND_M10	M10
C2	GND_C2	GND_N1	N1
C3	GND_C3	GND_N2	N2
C4	GND_C4	GND_N3	N3
C5	GND_C5	GND_N4	N4
C15	GND_C15	GND_N5	N5
D6	GND_D6	GND_N14	N14
D11	GND_D11	GND_N15	N15
E1	GND_E1	GND_P7	P7
E2	GND_E2	GND_P8	P8
E3	GND_E3	GND_P9	P9
E4	GND_E4	GND_P10	P10
E5	GND_E5	GND_P11	P11
E6	GND_E6	GND_P12	P12
E7	GND_E7	GND_R1	R1
E11	GND_E11	GND_R2	R2
E14	GND_E14	GND_R3	R3
E15	GND_E15	GND_R4	R4
F6	GND_F6	GND_R5	R5
G1	GND_G1	GND_R9	R9
G2	GND_G2	GND_R10	R10
G3	GND_G3	GND_R14	R14
G4	GND_G4	GND_R15	R15
G5	GND_G5	GND_T9	T9
G9	GND_G9	GND_T10	T10
G10	GND_G10	GND_U1	U1
G14	GND_G14	GND_U2	U2
G15	GND_G15	GND_U3	U3
H9	GND_H9	GND_U4	U4
H10	GND_H10	GND_U5	U5
J1	GND_J1	GND_U9	U9
J2	GND_J2	GND_U10	U10
J3	GND_J3	GND_U14	U14
J4	GND_J4	GND_U15	U15
J5	GND_J5	GND_W1	W1
J9	GND_J9	GND_W2	W2
J10	GND_J10	GND_W3	W3
J14	GND_J14	GND_W4	W4
J15	GND_J15	GND_W5	W5
K7	GND_K7	GND_W6	W6
K8	GND_K8	GND_W11	W11
K9	GND_K9	GND_W14	W14
K10	GND_K10	GND_W15	W15
K11	GND_K11	GND_Y6	Y6
K12	GND_K12	GND_Y11	Y11
L1	GND_L1	GND_Y13	Y13
L2	GND_L2	GND_AA1	AA1
L3	GND_L3	GND_AA2	AA2
L4	GND_L4	GND_AA3	AA3
L5	GND_L5	GND_AA4	AA4
L14	GND_L14	GND_AA5	AA5
L15	GND_L15	GND_AA14	AA14
M9	GND_M9	GND_AA15	AA15

HFB1M8MO331A0MR

U44007D

		DNU_A1	A1
		DNU_A2	A2
		DNU_A4	A4
		DNU_A6	A6
		DNU_A8	A8
		DNU_A11	A11
		DNU_A13	A13
		DNU_A15	A15
		DNU_A17	A17
		DNU_A18	A18
		DNU_B1	B1
		DNU_B2	B2
		DNU_B4	B4 — SMD RND 22.8mil GTP44020
		DNU_B8	B8
		DNU_B11	B11
		DNU_B13	B13
		DNU_B15	B15
		DNU_B17	B17
		DNU_B18	B18
		DNU_C6	C6
		DNU_C9	C9
		DNU_C11	C11
		DNU_C12	C12
		DNU/DDR_VDDQ	C16 — SMD RND 22.8mil GTP44021
		DNU_C17	C17 — SMD RND 22.8mil GTP44022
		DNU_C18	C18
		DNU_D12	D12
		DNU_E16	E16
		DNU_E17	E17
		DNU_E18	E18
		DNU_G16	G16
		DNU_G17	G17
		DNU_G18	G18
		DNU_J16	J16
		DNU_J17	J17
		DNU_J18	J18
		DNU_L16	L16
		DNU/JTAG_TRST#	L17
		DNU_N16	N16
		DNU_R16	R16
		DNU_U16	U16
		DNU_W16	W16
		DNU_W17	W17
C13	RFU_C13	DNU/SSD_FLUSH	Y7
C14	RFU_C14	DNU/SSD_FLUSH_FB	Y8
D15	RFU_D15	DNU_Y12	Y12
F15	RFU_F15	DNU_Y14	Y14
H14	RFU_H14	DNU_Y15	Y15
H15	RFU_H15	DNU_Y16	AA6
K14	RFU_K14	DNU_AA7	AA7
K15	RFU_K15	DNU_AA8	AA8
L7	RFU_L7	DNU_AA9	AA9
L8	RFU_L8	DNU_AA11	AA11
L9	RFU_L9	DNU_AA12	AA12
L10	RFU_L10	DNU_AA13	AA13
L11	RFU_L11	DNU_AA16	AA16
L12	RFU_L12	DNU/UART_RX	AA17
M7	RFU_M7	DNU/UART_TX	AA18 — SMD RND 22.8mil GTP44024 / SMD RND 22.8mil GTP44025
M8	RFU_M8	DNU_AB1	AB1
M11	RFU_M11	DNU_AB2	AB2
M12	RFU_M12	DNU_AB4	AB4
M14	RFU_M14	DNU_AB6	AB6
M15	RFU_M15	DNU_AB8	AB8
N7	RFU_N7	DNU_AB11	AB11
N8	RFU_N8	DNU_AB13	AB13
N9	RFU_N9	DNU_AB15	AB15
N10	RFU_N10	DNU/VCCF	AB17 — SMD RND 22.8mil GTP44027
N11	RFU_N11	DNU_AB18	AB18
N12	RFU_N12	DNU_AC1	AC1
P14	RFU_P14	DNU_AC2	AC2
P15	RFU_P15	DNU_AC4	AC4
T14	RFU_T14	DNU_AC6	AC6
T15	RFU_T15	DNU_AC8	AC8
V14	RFU_V14	DNU_AC11	AC11
V15	RFU_V15	DNU_AC13	AC13
W8	RFU_W8	DNU_AC15	AC15
W12	V_SEL0/RFU_W12	DNU/VCCFQ	AC17
W13	V_SEL1/RFU_W13	DNU_AC18	AC18 — SMD RND 22.8mil GTP44026 / SMD RND 22.8mil GTP44023

HFB1M8MO331A0MR

GTP44002 SMD RND 22.8mil

C44190 4.7u 6.3V 0201 DNP

V3P3_DSW

U44006 TPS62085RLTR QFN-7
VIN SW VOS FB GND PG
C44134 10u 6.3V 0402
C44139 0.1u 6.3V 0201 GND
L44102 0.47uH X950133-001 2.5X2.0X1.2
R44118 100K 1% 0201
3P3V_SSD
SMD RND 22.8mil GTP44015
R44018 82.5K 1% 0201 DNP
R44109 24.9K 1% 0201 SSD
C44141 100p 25V 0201 DNP
R44019 215K 1% 0201 DNP
R44110 165K 1% 0201 SSD
TP44007
MTP44026
C44035 22u 4V 20% 0603
DNP C44136 22u 4V 20% 0603
C44137 22u 4V 20% 0603
C44138 22u 4V 20% 0603
R44150 10K 0201 SSD
1P2V_SSD2

R44110 is 215K for Samsung, 1P2V_SSD = 1.06V-1.15V + 100mV P-P ripple
R44110 is 165K for Toshiba, 1P2V_SSD = 1.2V +/- 5%
R44110 is 165K and R44109 is 24.9K for Hynix, 1P2V_SSD = 0.92V +/- 0.08V
only support Hynix 1TB

3P3V_SSD
R44123 0 0201
R44119 100K 1% 0201
V3P3_DSW
R44134 100K 0201 GND
U44005 TPS62085RLTR QFN-7
VIN SW VOS FB GND PG
C44129 10u 6.3V 0402
C44180 0.1u 6.3V 0201 GND
L44101 0.47uH X950133-001 2.5X2.0X1.2
R44107 82.5K 1% 0201
C44140 100p 25V 0201 DNP
R44108 33K 1% 0201
R44124 33K 1% 0201
TP44006
MTP44027
C44130 22u 4V 20% 0603
C44131 22u 4V 20% 0603
C44132 22u 4V 20% 0603
C44133 22u 4V 20% 0603
1P8V_SSD2

1P2V_SSD2
U44007B HFB1M8MO331A0MR

G7	1p2v/1p1v/0p9v/RFU_G7	
G8	1p2v/1p1v/0p9v/RFU_G8	
G11	1p2v/1p1v/0p9v/RFU_G11	
G12	1p2v/1p1v/0p9v/RFU_G12	
H7	1p2v/1p1v/0p9v/RFU_H7	
H8	1p2v/1p1v/0p9v/RFU_H8	
H11	1p2v/1p1v/0p9v/RFU_H11	
H12	1p2v/1p1v/0p9v/RFU_H12	
J7	1p2v/1p1v/0p9v/RFU_J7	
J8	1p2v/1p1v/0p9v/RFU_J8	
J11	1p2v/1p1v/0p9v/RFU_J11	
J12	1p2v/1p1v/0p9v/RFU_J12	
R7	V1P8_R7	
R8	V1P8_R8	
R11	V1P8_R11	
R12	V1P8_R12	
T7	V1P8_T7	
T8	V1P8_T8	
T11	V1P8_T11	
T12	V1P8_T12	
U7	V1P8_U7	
U8	V1P8_U8	
U11	V1P8_U11	
U12	V1P8_U12	
D9	V3P3_D9	
D10	V3P3_D10	
E9	V3P3_E9	
E10	V3P3_E10	
W9	V3P3_W9	
W10	V3P3_W10	
Y9	V3P3_Y9	
Y10	V3P3_Y10	

1P8V_SSD2
3P3V_SSD

3VSUS_ORG
R44125 0201 49.9K SSD
R44017 0402 0 SSD
SSD2_SATA_PCIE_DET_N [24]
R44125 is loaded for non-RAID case
R44017 is loaded for the RAID case

3P3V_SSD
SSD C44107 6.3V 0.1u 0402 — SSD C44104 6.3V 1u 0402 — SSD C44105 0.1u 6.3V 0201 — SSD C44026 0.1u 6.3V 0201 — SSD C44108 6.3V 22u 0603 — SSD C44030 6.3V 22u 0603

1P8V_SSD2
SSD C44038 6.3V 1u 0402 — SSD C44028 6.3V 1u 0402 — SSD C44115 0.1u 6.3V 0201 — SSD C44109 0.1u 6.3V 0201 — SSD C44031 6.3V 22u 0603 — SSD C44033 6.3V 22u 0603

1P2V_SSD2
SSD C44025 6.3V 1u 0402 — SSD C44103 6.3V 1u 0402 — SSD C44024 0.1u 6.3V 0201 — SSD C44106 0.1u 6.3V 0201 — SSD C44113 0.1u 6.3V 0201 — SSD C44112 0.1u 6.3V 0201 — DNP C44114 6.3V 22u 0603 — SSD C44111 6.3V 22u 0603

U SPECIFIC

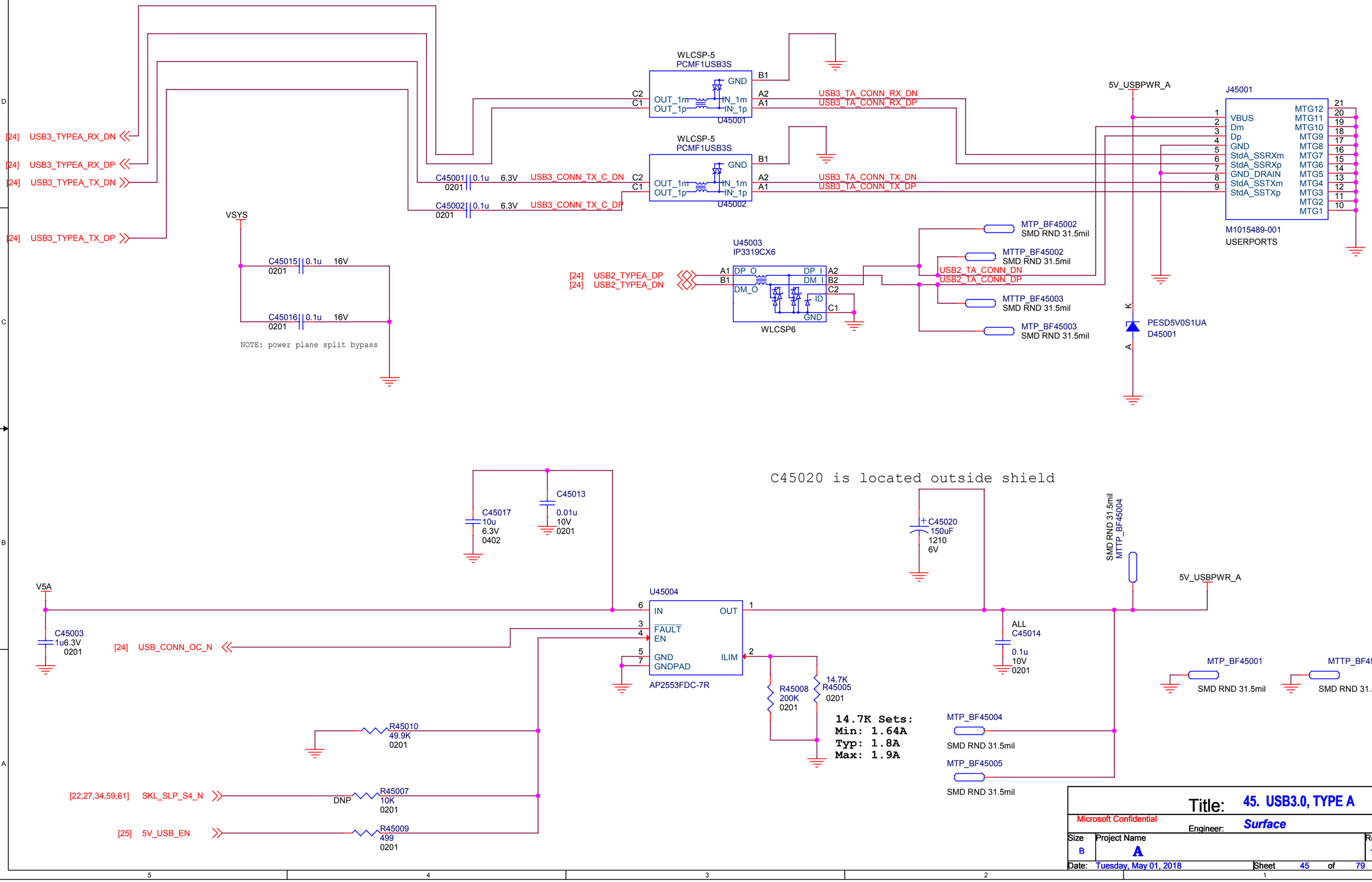
PCIE[12:1]_TXN/P : Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value, Gen3 = 176 to 265 nF; where 220 nF is nominal value

PCIE[12:1]_RXN/P : Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value, Gen3 = 176 to 265 nF; where 220 nF is nominal value

Difference between USB3 and PCIe: 1. No Choke, 2. Add cap on PER (p832 at DG v1.2)
RXN/RXP cap value must be different between Gen2 and Gen3
TX (from SOC) caps are at SOC side

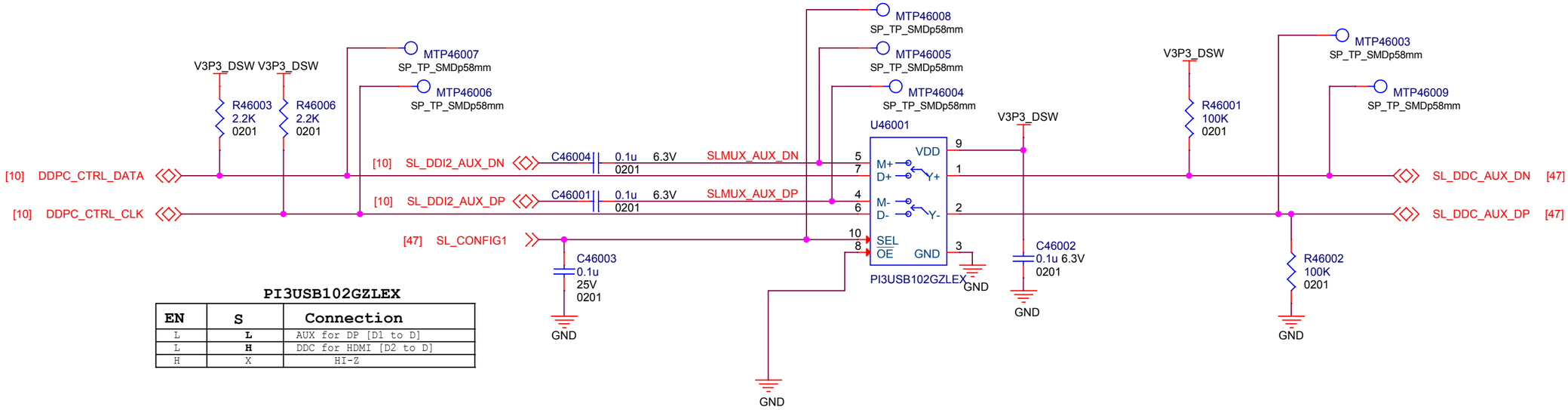
Always ON logic, as like Intel RVP5.

Title:	44. SSD Page 2	
Microsoft Confidential	Engineer:	Surface
Size: Custom	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 44 of 79	



Title:	45. USB3.0, TYPE A	
Microsoft Confidential	Engineer: Surface	
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Tuesday, May 01, 2018	Sheet 45 of 79	

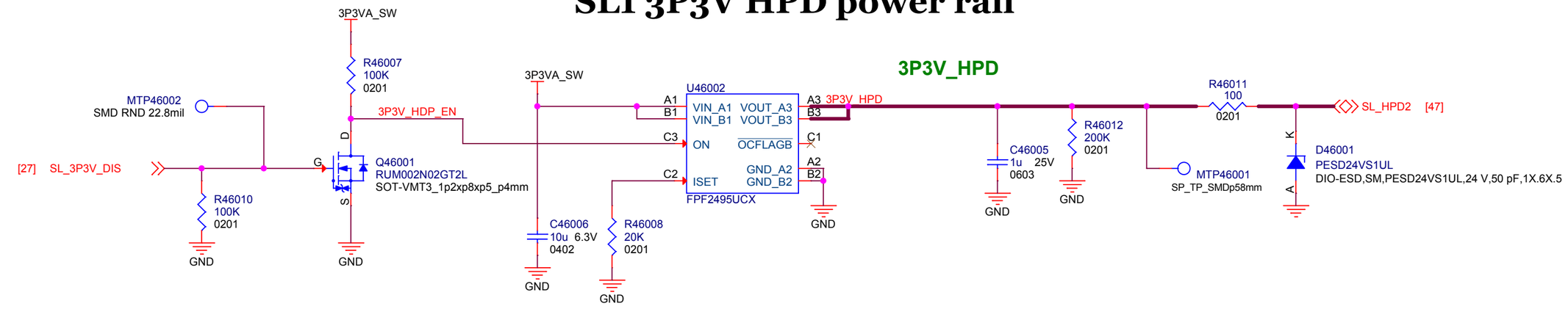
SL1 DP mux to HDMI/DVI Dongle control



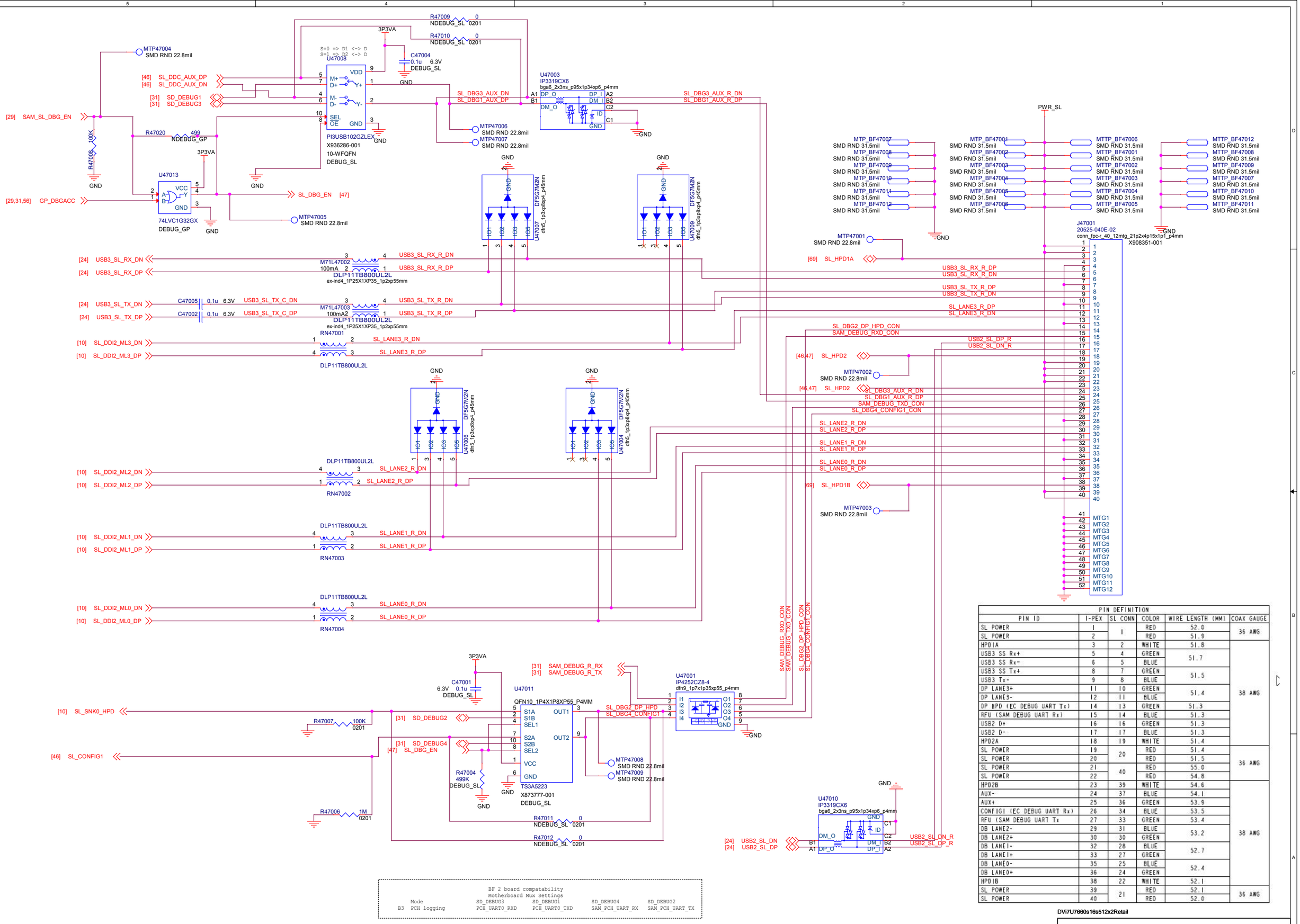
PI3USB102GZLEX

EN	S	Connection
L	L	AUX for DP [D1 to D]
L	H	DDC for HDMI [D2 to D]
H	X	HI-Z

SL1 3P3V HPD power rail



Title:	46. SL HDMI MUX/3P3V_HPD	
Engineer:	Surface	
Size: B	Project Name: A	Rev: 1.00
Date: Thursday, April 26, 2018	Sheet 46 of 76	



PIN DEFINITION					
PIN ID	I-PEX	SL CONN	COLOR	WIRE LENGTH (MM)	COAX GAUGE
SL POWER	1	1	RED	52.0	36 AWG
SL POWER	2		RED	51.9	
HPD1A	3	2	WHITE	51.8	38 AWG
USB3 SS Rx+	5	4	GREEN	51.7	
USB3 SS Rx-	6	5	BLUE		
USB3 SS Tx+	8	7	GREEN	51.5	
USB3 Tx-	9	8	BLUE		
DP LANE3+	11	10	GREEN	51.4	
DP LANE3-	12	11	BLUE		
DP HPD (EC DEBUG UART Tx)	14	13	GREEN	51.3	
RFU (SAM DEBUG UART Rx)	15	14	BLUE	51.3	
USB2 D+	16	16	GREEN	51.3	
USB2 D-	17	17	BLUE	51.3	
HPD2A	18	19	WHITE	51.4	
SL POWER	19	20	RED	51.4	36 AWG
SL POWER	20		RED	51.5	
SL POWER	21	40	RED	55.0	
SL POWER	22		RED	54.8	
HPD2B	23	39	WHITE	54.6	38 AWG
AUX-	24	37	BLUE	54.1	
AUX+	25	36	GREEN	53.9	
CONFIG1 (EC DEBUG UART Rx)	26	34	BLUE	53.5	
RFU (SAM DEBUG UART Tx	27	33	GREEN	53.4	
DB LANE2-	29	31	BLUE	53.2	
DB LANE2+	30	30	GREEN		
DB LANE1-	32	28	BLUE	52.7	
DB LANE1+	33	27	GREEN		
DB LANE0-	35	25	BLUE	52.4	
DB LANE0+	36	24	GREEN		
HPD1B	38	22	WHITE	52.1	
SL POWER	39	21	RED	52.1	36 AWG
SL POWER	40		RED	52.0	

BF 2 board compatability Motherboard Mux Settings				
Mode	SD_DEBUG3	SD_DEBUG1	SD_DEBUG4	SD_DEBUG2
B3 PCH logging	PCH_UART0_RXD	PCH_UART0_TXD	SAM_PCH_UART_RX	SAM_PCH_UART_TX

DVi7U7660s16s512x2Retail

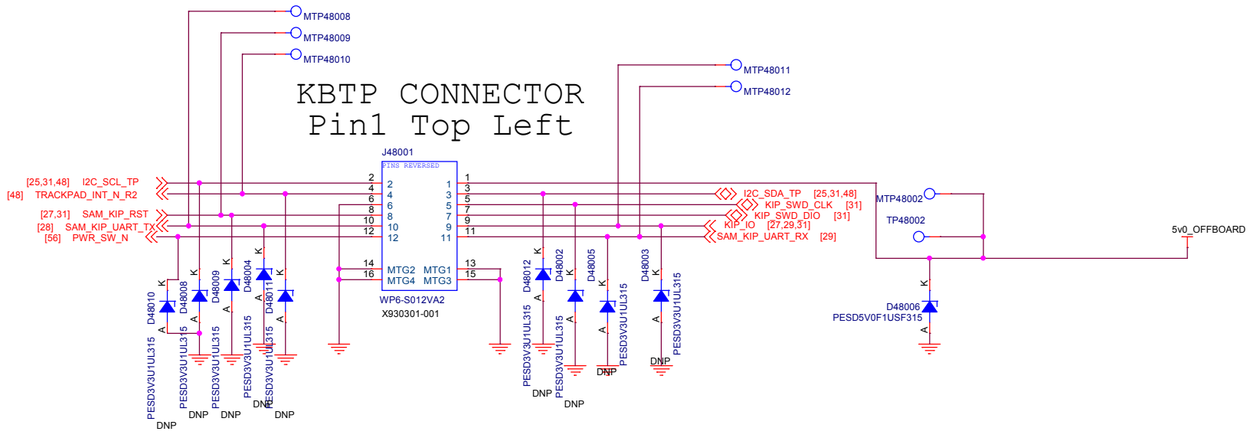
Microsoft Confidential

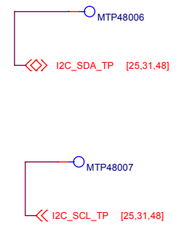
Title: 47. SurfLink Connector

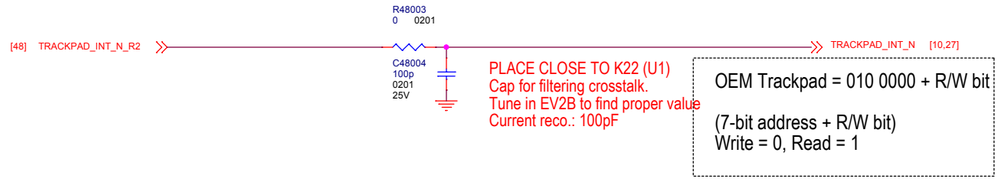
Engineer:

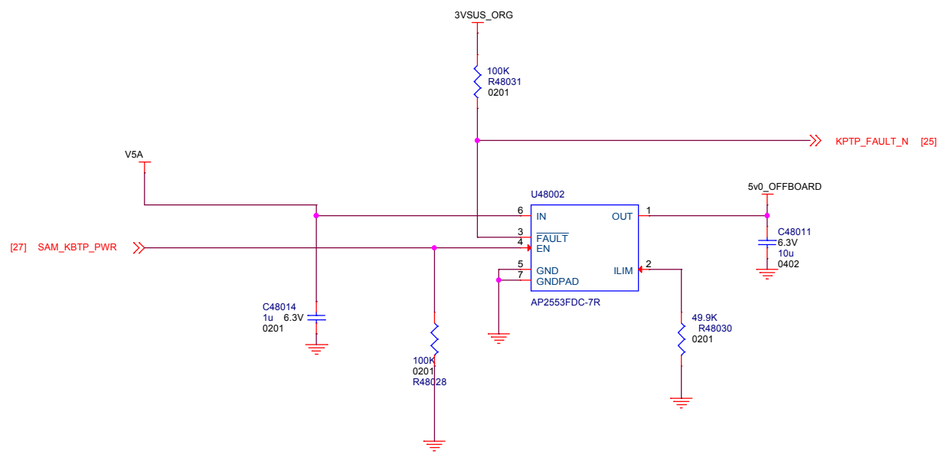
Size	Project Name	Rev
C	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 47 of XX









Title: 48. Blade			
Microsoft Confidential	Engineer: Surface		
Size: Custom A	Project Name		Rev: 1.0.0.1
Date: Thursday, April 26, 2018		Sheet 48 of 79	

[25,49] TPANEL_RST_N
TPANEL_RST_N
TS_V1P0_TCH_DIG
1P8V_TS
C49004 2.2u 6.3V
C49059 0.1u
C49060 100p
C49008 2.2u 6.3V
C49061 0.1u
C49062 100p
C49085 10u
TS_V1P0_TCH_SSI
C49006 2.2u 6.3V
C49063 0.1u
C49064 100p
C49005 2.2u 6.3V
C49065 0.1u
C49066 100p
3VSUS_ORG
R49029 100K
[21,49] TS_SPI_CLK
[21,49] TS_SPI_MOSI
[21,49] TS_SPI_MISO
[21,49] TS_SPI_CS_N
[30] TS_IRQ_3V3_N
R49014 22.1
TS_TOUCH_SPI_DO_3V3
Q49007
NX3008NBKW,MB315
MTP49048
GTP49003
TS_GPIO0
TS_IRQ_1V8
[20,49] FLASH_PROTECT_N
R49016 1K
TS_FLASH_PROTECTn_GPIO_C
R49030 10K
U49001
SPI_CLK/I2C_SCL
SPI_DI / I2C_SDA
GPIO7 / SPI_DO
GPIO6 / SPI_CS
GPIO0
GPIO1 / INT
GPIO2 / IF_SEL
GPIO3
GPIO4
GPIO5
GPIO9
GPIO10
GPIO11
TCK
TDI
TDO
TMS
CLK_IN
XI
XO
CLK_SLCT
FSCK
FSDI
FSDIO
FSCS
VDD_SSI
VDD_CORE
VDE_H
VDE_F
RESERVED_GND[0]
RESERVED_GND[1]
RESERVED_GND[2]
RESERVED_GND[3]
RESERVED_GND[4]
RESERVED_GND[5]
RESERVED_GND[6]
RESERVED_GND[7]
RESERVED_GND[8]
RESERVED_GND[9]
RESERVED_NC[0]
RESERVED_NC[1]
RESERVED_NC[2]
RESERVED_NC[3]
RESERVED_NC[4]
RESERVED_NC[5]
RESERVED_NC[6]
RSTN_D
VDD_OK_F
RSTN
SCKL
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
GND1
GND2
DS-D5000-B064
GPIO signals may toggle during boot (see errata document). Please make sure to implement the workaround described in the errata
[31,49] TS_TCK_1V8
[31,49] TS_TDI_1V8
[31,49] TS_TDO_1V8
[31,49] TS_TMS_1V8
R49017 22.1 0201
TS_JTAG_TS_TDO_R
TS_HOST_CLK (If Available)
R49018 200K
TS_DLITE_XI
TS_DLITE_XO_R
R49015 0 0201
Y49001 3_TS_DLITE_XO
XTAL-XTAL,SM,48 MHZ,15 PPM,7 PF,2X1.6X0.155MM
48MHz
C49016 12p 25V 2%
C49017 12p 25V 2%
The crystal and capacitors should be placed as close as possible to the D5, with short and symmetrical traces to the XI and XO pins
TS_FLASH_SCK
TS_FLASH_MISO
TS_FLASH_MOSI
TS_FLASH_CS#
1P8V_TS
U49003 son9_4x4xp6_p8mm
CS
CK
SI/0
Q/1
WP/2
HLRS/3
VCC
MTG
VSS
MX25U1635FZUI
C49019 2.2u 16V
Special keepout made to isolate buck and boost ground from system ground
MTP49049
MTP49051
MTP49040
MTP49041
MTP49044
MTP49045
MTP49046
1P8V_TS
R49024 200K DNP
FLASH_PROTECT_N
FLASH_PROTECT_N [20,49]
5V_TS
1P8V_TS
MTP49042
MTP49014
MTP49027
MTP49008
TPANEL_RST_N
FLASH_PROTECT_N
TPANEL_RST_N [25,49]
FLASH_PROTECT_N [20,49]
TS_TCK_1V8
TS_TMS_1V8
TS_TDO_1V8
TS_TDI_1V8
MTP49016
MTP49022
MTP49023
MTP49017
[31,49]
Not to be used for DEBUG build
Use MTP points on pg 31 instead
TS_SPI_CLK
TS_SPI_MISO
TS_SPI_MOSI
TS_SPI_CS_N
MTP49024
MTP49025
MTP49018
MTP49019
[21,49]
MTP49015
X950113-001
L49003 0.47uH 0805
1P8V_TS
C49052 10u 6.3V 0603
C49021 10u 6.3V 0603
C49020 10u 6.3V 0603
TS_V1P8A
MTP49032
V1P8 Analog
5V_TS
MTP49035
MTP49038
TS_HV_IN
C49007 10u 25V 0603
C49002 2.2u 25V 0402
C49067 0.1u 25V 0201
C49055 100p 0201
C49035 0.1u 16V
C49036 100p
C49003 10u 6.3V 0603
TS_BOOST_HV_IN
L49001 2.2uH 1.4A 2.0X1.6X1.0MM
C49007 10u 0603
1P8V_TS
TS_V1P0_TCH_DIG
L49002 4.7uH 0805
C49009 10u 6.3V 0603
TS_V1P0_TCH_SSI
C49010 4.7u 0402
C49011 2.2u 0402
C49070 0.1u 0201
C49058 100p 0201
1P8V_TS
TS_V1P8A
C49012 2.2u 0402
C49071 0.1u 0201
C49072 100p 0201
C49032 4.99K 0402
C49068 0.1u 0201
C49069 100p 0201
TPANEL_RST_N
C49013 0.1u 0201
C49014 0.033u 0201
C49015 0.033u 0201
1P8V_TS
TS_AY_RSTN_D
TS_VDD_OK_F
TS_VDD_OK_H
MTP49047
TS_SCKL
TS_SD0
TS_SD1
TS_SD2
TS_SD3
MTP49003
MTP49004
MTP49005
MTP49006
TS_SCKL
TS_SD0
TS_SD4
TS_SD8
U49002
HV_IN
BOOST_HV_OUT
BOOST_HV_IN
BOOST_VSS
BUCK_1V8_IN
BUCK_VSS
BUCK_OUT_FB
BUCK_LX
VDD_SSI
LDO_1V0_OUT
VDD_1V8_IN
AVDD_IN
AVDD_1V8_3
AVDD_1V8_2
AVDD_1V8_1
VDE_H
VDE_F
RSTN_H
RSTN_D
VDD_OK_F
VDD_OK_H
SCLK
A5_SSI_D0
A5_SSI_D1
A5_SSI_D2
A5_SSI_D3
GND
ATB
ANT_HV0
ANT_HV1
ANT_HV2
ANT_HV3
ANT_HV4
ANT_HV5
ANT_HV6
ANT_HV7
ANT_HV8
ANT_HV9
ANT_HV10
ANT_HV11
ANT_HV12
ANT_HV13
ANT_HV14
ANT_HV15
ANT_HV16
ANT_HV17
ANT_HV18
ANT_HV19
ANT_HV20
ANT_HV21
ANT_HV22
ANT_HV23
ANT_LV0
ANT_LV1
ANT_LV2
ANT_LV3
ANT_LV4
ANT_LV5
ANT_LV6
ANT_LV7
ANT_LV8
ANT_LV9
ANT_LV10
ANT_LV11
ANT_LV12
ANT_LV13
ANT_LV14
ANT_LV15
ANT_LV16
ANT_LV17
ANT_LV18
ANT_LV19
ANT_LV20
ANT_LV21
ANT_LV22
ANT_LV23
TS_AY0_ANT_LV0
TS_AY0_ANT_LV1
TS_AY0_ANT_LV2
TS_AY0_ANT_LV3
TS_AY0_ANT_LV4
TS_AY0_ANT_LV5
TS_AY0_ANT_LV6
TS_AY0_ANT_LV7
TS_AY0_ANT_LV8
TS_AY0_ANT_LV9
TS_AY0_ANT_LV10
TS_AY0_ANT_LV11
TS_AY0_ANT_LV12
TS_AY0_ANT_LV13
TS_AY0_ANT_LV14
TS_AY0_ANT_LV15
TS_AY0_ANT_LV16
TS_AY0_ANT_LV17
TS_AY0_ANT_LV18
TS_AY0_ANT_LV19
TS_AY0_ANT_LV20
TS_AY0_ANT_LV21
TS_AY0_ANT_LV22
TS_AY0_ANT_LV23
RESERVED_GND1
RESERVED_GND2
RESERVED_GND3
RESERVED_NC1
RESERVED_NC2
RESERVED_NC3
MTP49001
DS-A5048_82BGA
Add underfill
U49004
TS_AY1_ANT_HV0
TS_AY1_ANT_HV1
TS_AY1_ANT_HV2
TS_AY1_ANT_HV3
TS_AY1_ANT_HV4
TS_AY1_ANT_HV5
TS_AY1_ANT_HV6
TS_AY1_ANT_HV7
TS_AY1_ANT_HV8
TS_AY1_ANT_HV9
TS_AY1_ANT_HV10
TS_AY1_ANT_HV11
TS_AY1_ANT_HV12
TS_AY1_ANT_HV13
TS_AY1_ANT_HV14
TS_AY1_ANT_HV15
TS_AY1_ANT_HV16
TS_AY1_ANT_HV17
TS_AY1_ANT_HV18
TS_AY1_ANT_HV19
TS_AY1_ANT_HV20
TS_AY1_ANT_HV21
TS_AY1_ANT_HV22
TS_AY1_ANT_HV23
TS_AY1_ANT_LV0
TS_AY1_ANT_LV1
TS_AY1_ANT_LV2
TS_AY1_ANT_LV3
TS_AY1_ANT_LV4
TS_AY1_ANT_LV5
TS_AY1_ANT_LV6
TS_AY1_ANT_LV7
TS_AY1_ANT_LV8
TS_AY1_ANT_LV9
TS_AY1_ANT_LV10
TS_AY1_ANT_LV11
TS_AY1_ANT_LV12
TS_AY1_ANT_LV13
TS_AY1_ANT_LV14
TS_AY1_ANT_LV15
TS_AY1_ANT_LV16
TS_AY1_ANT_LV17
TS_AY1_ANT_LV18
TS_AY1_ANT_LV19
TS_AY1_ANT_LV20
TS_AY1_ANT_LV21
TS_AY1_ANT_LV22
TS_AY1_ANT_LV23
MTP49002
DS-A5048_82BGA
Add underfill
U49005
TS_AY2_ANT_HV0
TS_AY2_ANT_HV1
TS_AY2_ANT_HV2
TS_AY2_ANT_HV3
TS_AY2_ANT_HV4
TS_AY2_ANT_HV5
TS_AY2_ANT_HV6
TS_AY2_ANT_HV7
TS_AY2_ANT_HV8
TS_AY2_ANT_HV9
TS_AY2_ANT_HV10
TS_AY2_ANT_HV11
TS_AY2_ANT_HV12
TS_AY2_ANT_HV13
TS_AY2_ANT_HV14
TS_AY2_ANT_HV15
TS_AY2_ANT_HV16
TS_AY2_ANT_HV17
TS_AY2_ANT_HV18
TS_AY2_ANT_HV19
TS_AY2_ANT_HV20
TS_AY2_ANT_HV21
TS_AY2_ANT_HV22
TS_AY2_ANT_HV23
TS_AY2_ANT_LV0
TS_AY2_ANT_LV1
TS_AY2_ANT_LV2
TS_AY2_ANT_LV3
TS_AY2_ANT_LV4
TS_AY2_ANT_LV5
TS_AY2_ANT_LV6
TS_AY2_ANT_LV7
TS_AY2_ANT_LV8
TS_AY2_ANT_LV9
TS_AY2_ANT_LV10
TS_AY2_ANT_LV11
TS_AY2_ANT_LV12
TS_AY2_ANT_LV13
TS_AY2_ANT_LV14
TS_AY2_ANT_LV15
TS_AY2_ANT_LV16
TS_AY2_ANT_LV17
TS_AY2_ANT_LV18
TS_AY2_ANT_LV19
TS_AY2_ANT_LV20
TS_AY2_ANT_LV21
TS_AY2_ANT_LV22
TS_AY2_ANT_LV23
MTP49003
DS-A5048_82BGA
Add underfill
Title: 49. Touch
Microsoft Confidential
Engineer: Surface
Size Custom
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
Sheet 49 of 76
50 pin Drive Connector
J49002
TS_AY1_ANT_HV1
TS_AY1_ANT_HV3
TS_AY1_ANT_HV5
TS_AY1_ANT_HV7
TS_AY1_ANT_HV9
TS_AY1_ANT_HV11
TS_AY1_ANT_HV13
TS_AY1_ANT_HV15
TS_AY1_ANT_HV17
TS_AY1_ANT_HV19
TS_AY1_ANT_HV21
TS_AY1_ANT_HV23
TS_AY2_ANT_HV1
TS_AY2_ANT_HV3
TS_AY2_ANT_HV5
TS_AY2_ANT_HV7
TS_AY2_ANT_HV9
TS_AY2_ANT_HV11
TS_AY2_ANT_HV13
TS_AY2_ANT_HV15
TS_AY2_ANT_HV17
TS_AY2_ANT_HV19
TS_AY2_ANT_HV21
TS_AY2_ANT_HV23
TS_AY1_ANT_HV0
TS_AY1_ANT_HV2
TS_AY1_ANT_HV4
TS_AY1_ANT_HV6
TS_AY1_ANT_HV8
TS_AY1_ANT_HV10
TS_AY1_ANT_HV12
TS_AY1_ANT_HV14
TS_AY1_ANT_HV16
TS_AY1_ANT_HV18
TS_AY1_ANT_HV20
TS_AY1_ANT_HV22
TS_AY2_ANT_HV0
TS_AY2_ANT_HV2
TS_AY2_ANT_HV4
TS_AY2_ANT_HV6
TS_AY2_ANT_HV8
TS_AY2_ANT_HV10
TS_AY2_ANT_HV12
TS_AY2_ANT_HV14
TS_AY2_ANT_HV16
TS_AY2_ANT_HV18
TS_AY2_ANT_HV20
TS_AY2_ANT_HV22
V48
MTG1 MTG2 MTG3 MTG4
5024265010
50 pin Flex Breakout
H0 to H47 are the horizontal sensor traces
V0 to V71 are the vertical sensor lines
80 pin Sense Connector
J49003
TS_AY2_ANT_LV6
TS_AY2_ANT_LV4
TS_AY2_ANT_LV2
TS_AY2_ANT_LV0
TS_AY2_ANT_LV14
TS_AY2_ANT_LV12
TS_AY2_ANT_LV10
TS_AY2_ANT_LV8
TS_AY2_ANT_LV22
TS_AY2_ANT_LV20
TS_AY2_ANT_LV18
TS_AY2_ANT_LV16
TS_AY1_ANT_LV6
TS_AY1_ANT_LV4
TS_AY1_ANT_LV2
TS_AY1_ANT_LV0
TS_AY1_ANT_LV14
TS_AY1_ANT_LV12
TS_AY1_ANT_LV10
TS_AY1_ANT_LV8
TS_AY1_ANT_LV22
TS_AY1_ANT_LV20
TS_AY1_ANT_LV18
TS_AY1_ANT_LV16
TS_AY0_ANT_LV6
TS_AY0_ANT_LV4
TS_AY0_ANT_LV2
TS_AY0_ANT_LV0
TS_AY0_ANT_LV14
TS_AY0_ANT_LV12
TS_AY0_ANT_LV10
TS_AY0_ANT_LV8
TS_AY0_ANT_LV22
TS_AY0_ANT_LV20
TS_AY0_ANT_LV18
TS_AY0_ANT_LV16
TS_AY2_ANT_LV7
TS_AY2_ANT_LV5
TS_AY2_ANT_LV3
TS_AY2_ANT_LV1
TS_AY2_ANT_LV15
TS_AY2_ANT_LV13
TS_AY2_ANT_LV11
TS_AY2_ANT_LV9
TS_AY2_ANT_LV23
TS_AY2_ANT_LV21
TS_AY2_ANT_LV19
TS_AY2_ANT_LV17
TS_AY1_ANT_LV7
TS_AY1_ANT_LV5
TS_AY1_ANT_LV3
TS_AY1_ANT_LV1
TS_AY1_ANT_LV15
TS_AY1_ANT_LV13
TS_AY1_ANT_LV11
TS_AY1_ANT_LV9
TS_AY1_ANT_LV23
TS_AY1_ANT_LV21
TS_AY1_ANT_LV19
TS_AY1_ANT_LV17
TS_AY0_ANT_LV7
TS_AY0_ANT_LV5
TS_AY0_ANT_LV3
TS_AY0_ANT_LV1
TS_AY0_ANT_LV15
TS_AY0_ANT_LV13
TS_AY0_ANT_LV11
TS_AY0_ANT_LV9
TS_AY0_ANT_LV23
TS_AY0_ANT_LV21
TS_AY0_ANT_LV19
TS_AY0_ANT_LV17
V0 V1 V2 V3 V4 V5 V6 V7 V8 V9 V10 V11 V12 V13 V14 V15 V16 V17 V18 V19 V20 V21 V22 V23 V24 V25 V26 V27 V28 V29 V30 V31 V32 V33 V34 V35 V36 V37 V38 V39 V40 V41 V42 V43 V44 V45 V46 V47 V48 V49 V50 V51 V52 V53 V54 V55 V56 V57 V58 V59 V60 V61 V62 V63 V64 V65 V66 V67 V68 V69 V70 V71
MTG1 MTG2 MTG3 MTG4
5024268010
80 pin Flex Breakout

1P8V_WIFI_INT_OUT
VDD1V8_RF_K9
C50003 1u 6.3V 0201
C50005 3.3p 25V 0201
VDD1V8_RF_K3
C50007 1u 6.3V 0201
C50008 100p 25V 0201
VDD1V8_RF_J1
C50010 100p 25V 0201
VDD1V8_RF_H1
C50013 100p 25V 0201
VDD1V8_RF_G1
C50014 1u 6.3V 0201
VDD1V8_RF_F1
C50023 0.1u 6.3V 0201
VDD1V8_RF_M14
C50029 2.2u 6.3V 0402
C50030 100p 25V 0201
VDD1V8_RF_NFC_E14
C50034 0.1u 6.3V 0201
1P8V_WIFI_INT_OUT
VDD1V8_RF_H16
C50001 100p 25V 0201
VDD1V8_RF_K16
C50002 100p 25V 0201
VDD1V8_RF_G16
C50006 100p 25V 0201
VDD1V8_RF_D2
C50011 100p 25V 0201
VDD1V8_RF_C1
C50012 100p 25V 0201
VDD1V8_RF_PCIE_HSIC_A10
C50016 1u 6.3V 0201
C50017 10p 50V 0201
3P3V_RADIO
VDD3V3_RF_M3
C50026 10u 6.3V 0603
C50027 100p 25V 0201
C50028 3.3p 25V 0201
VDD3V3_RF_M9
C50031 10u 6.3V 0603
C50032 100p 25V 0201
C50033 3.3p 25V 0201
VDD3V3_RF_B11
C50035 1u 6.3V 0201
C50037 0.1u 6.3V 0201
VIO_RF_L12
C50039 0.1u 6.3V 0201
3P3V_RADIO
R50042 10K 0201 PCIE_WIFI_CLKREQ_N [20,50]
R50036 10K 0201 PCIE_WIFI_WAKE_N [25,50]
R50037 DNP 49.9K 0201
3P3V_RADIO
R50038 DNP 10K 0201
R50039 49.9K 0201 PCIE_WIFI_DISABLE_N [25,50]
R50040 DNP 10K 0201
R50041 49.9K 0201 PCIE_WIFI_PERST_N [25,50]
1P8V_WIFI_INT_OUT
U50001A
A10 AVDD18_1
J1 AVDD18_10
K3 AVDD18_11
K9 AVDD18_12
K16 AVDD18_13
M14 AVDD18_14
C1 AVDD18_2
D2 AVDD18_3
E14 AVDD18_4
F1 AVDD18_5
G1 AVDD18_6
G16 AVDD18_7
H1 AVDD18_8
H16 AVDD18_9
B11 AVDD33_1
D16 AVDD33_2
M3 AVDD33_3
M9 AVDD33_4
D15 AVSS1
H10 AVSS10
H15 AVSS11
J15 AVSS12
J16 AVSS13
K1 AVSS14
K15 AVSS15
L2 AVSS16
L3 AVSS17
L5 AVSS18
L7 AVSS19
F2 AVSS2
L9 AVSS20
L10 AVSS21
L13 AVSS22
L16 AVSS23
F3 AVSS3
F16 AVSS4
G2 AVSS5
G15 AVSS6
H2 AVSS7
H3 AVSS8
H9 AVSS9
88W8897-B1-CBK2-T
3P3V_RADIO
MTTP50004 SMD RND 22.8mil
VDD3V3_RF_D16
C50009 6.3V 0.1u 0201
C50070 2p 25V 0201
C50071 2p 25V 0201
GPIO[0] C3 WIFI_GPIO0 MTTP50001 SMD RND 22.8mil
GPIO[1] D5 WIFI_GPIO1 MTTP50002 SMD RND 22.8mil
GPIO[2] B2 WIFI_GPIO2 MTTP50003
GPIO[3] A3
GPIO[4] E7
GPIO[5] E8
GPIO[6] E9
GPIO[7] E10
GPIO[8]/LED_OUT_WLAN K13
GPIO[9]/LED_OUT_BT J13
GPIO[10]/SER_WB E6
GPIO[11]/LED_OUT_NFC E11
GPIO[12]/PCIE_PERSTn D8 PCIE_W_PERST_N
GPIO[13]/PCIE_W_DISABLE B7 PCIE_W_DISABLE
GPIO[14] B6
GPIO[15] A5
GPIO[16] D6
GPIO[17] B5
GPIO[18] C6
GPIO[19] C4
GPIO[20] C5
GPIO[21] B3
GPIO[22] B4
GPIO[23] C2
GPIO[24] D4
CONFIG_HOST[0] G5 WF_CNFG_HST0 MTTP50005 SMD RND 22.8mil
CONFIG_HOST[1] E5 WF_CNFG_HST1 MTTP50006 SMD RND 22.8mil
CONFIG_HOST[2] F4 WF_CNFG_HST2 MTTP50007 SMD RND 22.8mil
CONFIG_HOST[3] E4 WF_CNFG_HST3 MTTP50008 SMD RND 22.8mil
BRF_ANT M15 BRF_ANT_M15 [50]
BUCK11_SENSE B14
BUCK11_VOUT A15 WF_BUCK11_VOUT
L50002 2.2uH 2.5X2X1.2MM 1.67A
BUCK18_SENSE C15
BUCK18_VOUT B16 WF_BUCK18_VOUT
L50003 2.2uH 2.5X2X1.2MM 1.67A
C50024 10u 6.3V 0603
SMD RND 22.8mil
DNP C50004 0.1u 6.3V 0201
PCIE_W_PERST_N 220 0201 R50001 PCIE_WIFI_PERST_N [25,50]
PCIE_W_DISABLE 0 0201 R50002 PCIE_WIFI_DISABLE_N [25,50]
1P1V_WIFI_INT 1.1V R50003 0 0201 1P1V_WIFI_INT_OUT
1P8V_WIFI_INT 1.8V R50006 0 0201 1P8V_WIFI_INT_OUT
1P8V_WIFI_INT_OUT
R50005 49.9K 0201
R50007 49.9K 0201
R50008 49.9K 0201
R50009 49.9K 0201
C50015 10u 6.3V 0603
1P1V_WIFI_INT
3P3V_WWAN
C50018 0.1u 6.3V 0201
L50001 0402 2.2A 30 OHM 30 Ohm
3P3V_RADIO
C50020 10u 6.3V 0603
C50021 0.1u 6.3V 0201
OPTION HOST VIO
1P8V_WIFI_INT_OUT
3P3V_RADIO
DNP R50014 0 0201
R50015 0 0201
VIO
VIO
C50036 0.1u 6.3V 0201
WIFI > PCIe3
[20,50] PCIE_WIFI_CLKREQ_N R50021 0 0201 PCIE_WIFI_CLKREQ_N_R
[20] PCIE_WIFI_RCLK_DN R50022 0 0201 PCIE_WIFI_RCLK_R_DN
[20] PCIE_WIFI_RCLK_DP R50023 0 0201 PCIE_WIFI_RCLK_R_DP
[24] PCIE_WIFI_TX9_DN
[24] PCIE_WIFI_TX9_DP
[24] PCIE_WIFI_RX9_DN C50045 0.1u 6.3V 0201 PCIE_WIFI_C_RX9_DN
[24] PCIE_WIFI_RX9_DP C50046 0.1u 6.3V 0201 PCIE_WIFI_C_RX9_DP
[25,50] PCIE_WIFI_WAKE_N R50024 0 0201 PCIE_WAKE_N_R
[25] WLAN_PWD_N R50025 0 0201
SMD RND 31.5mil MTP_BF50001 M_PDN
SMD RND 31.5mil MTP_BF50002 AT0
SMD RND 31.5mil MTP_BF50003
R50027 49.9K 0201
Done: RF_CNTL0_N = 1 for 40MHz auto calibration
RF_CNTL0_N G9
RF_CNTL1_P G10
RF_TR_2_A M5
RF_TR_2_B M10
RF_TR_5_A M2
RF_TR_5_B M7
SD_CLK B12
SD_CMD C12
88W8897-B1-CBK2-T
U50001B
RES_D10 D10
RES_C10 C10
NFC_ANT_N E15
NFC_ANT_P E16
NFC_SWP1_IO F13
NFC_SWP1_VDDIN F14
NFC_SWP1_VDDOUT F15
NFC_SWP2_IO F12
NFC_SWP2_VDDOUT E13
NFC_TWSI_CLK G14
NFC_TWSI_SDA G13
NFC_VDDANT E12
NFC_WI_IN G12
PCIE_CLKREQn C7
PCIE_RCLK_N D9
PCIE_RCLK_P C8
PCIE_RX_N C9
PCIE_RX_P B9
PCIE_TX_N B8
PCIE_TX_P A8
PCIE_WAKEn D7
PDn D13
RES1 D14
RES10 H11
RES11 H12
RES12 J12
RES13 K12
RES2 F8
RES3 F9
RES4 F10
RES5 F11
RES6 G4
RES7 G7
RES8 G8
RES9 G11
C50038 0.1u 6.3V 0201 NFC_SWP1_VDDIN
TCK J14
TDI H14
TDO H13
TMS L14
USB_DMNS D11
USB_DPLS C11
VBAT_IN B15
VBLDO33_CNTL F7
VBLDO33_SENSE F6
VDD11 A7
VDD12 B10
VIO A2
VIO_RF L12
VIO_SD A12
VSS1 A6
VSS2 A9
VSS3 A11
VSS4 A14
VSS5 B1
VSS6 C14
VSS7 C16
VSS8 D1
XTAL_IN E1 REF_CLK_IN
XTAL_OUT E2 REF_CLK_OUT
SLP_CLK_IN A4
SER_DAT E3 SER_DAT
SER_CSn F5 SER_CSN
SER_CLK D3 SER_CLK
SD_DAT[0] D12
SD_DAT[1] C13
SD_DAT[2] B13
SD_DAT[3] A13
MTTP50009 SMD RND 22.8mil PLACE TP's on BOTTOM,
MTTP50010 SMD RND 22.8mil
MTTP50011 SMD RND 22.8mil
MTTP50012 SMD RND 22.8mil
3P3V_RADIO
R50016 49.9K 0201
R50017 49.9K 0201 DNP
BT -> USB2.0(5)
USB_DMNS R50018 0 0201 USB2_BT_DN [24]
USB_DPLS R50019 0 0201 USB2_BT_DP [24]
WF_VBAT_IN_3V3
3P3V_RADIO
R50020 0 0201
1P1V_WIFI_INT_OUT
C50041 1u 6.3V 0201
C50040 10u 6.3V 0603
C50042 0.1u 6.3V 0201 DNP GND VIO
C50047 0.1u 6.3V 0201
3P3V_RADIO
VIO
MTTP50013 SMD RND 22.8mil
1P8V_WIFI_INT_OUT
SER_CSN R50028 49.9K 0201
R50029 49.9K 0201 DNP
MTTP50014 SMD RND 22.8mil
MTTP50015 SMD RND 22.8mil
Y50001 FL4000023 3.2X2.5MM
MTTP50016 SMD RND 22.8mil
1P8V_WIFI_INT_OUT
R50031 10K 0201
R50032 10K 0201
C50057 0.1u 6.3V 0201
U50003 AT24C16D-MAHM
NC 1
NC1 2
NC2 3
GND 4
PAD 9
Vcc 8
WP 7 WF_EEP_WP
SCL 6 SER_CLK
SDA 5 SER_DAT
X912618-001
EEPROM
P50001 SMA GND 2,3,4
WF_RF_PATH_A_ANT
20449-001E
X864717-001
J50001 MM8030-2610RK0 PROBE OUT IN GND3GND4
WF_RF_PATH_COAX
U50002 LFD182G45MJ6D431 GND1 5G_IN ANT GND GND3 2G_IN
DNP C50050 5.6p 0201
RF_TR_5_A_C C50054 5.6p 0201 25V RF_TR_5_A
WIFI_RF_2_A_OUT C50055 10p 0201 50V RF_TR_2_A
DNP C50056 5.6p 0201 25V
L50006 LXES15AAA1-153 X935756-001
Done: 4.7k 0402 for ESD
P50002 SMA GND 2,3,4
WF_RF_PATH_B_ANT
20449-001E
X864717-001
J50002 MM8030-2610RK0 PROBE OUT IN GND3GND4
WF_RF_PATH_B
L50009 LXES15AAA1-153 X935756-001
U50004 LFD182G45MJ6D431 GND1 5G_IN ANT GND GND3 2G_IN
GND
C50058 5.6p 0201 25V DNP
RF_TR_5_B_C C50063 5.6p 0201 25V RF_TR_5_B
WIFI_RF_2_B_FIL_IN
3P3V_RADIO
R50030 49.9K 0201
3P3V_RADIO
R50033 0 0201
C50060 10p 0201 50V <HDL_POWER>
U50005 BGS12SN6 VDD RFIN CTRL GND RF1 RF2
C50066 10p 50V 0201 WIFI_RF_2_B_FIL_IN_C
R50034 0 0201
RF_CNTL1_P_R
C50069 10p 50V 0201
RF_TR_2_B_1 C50065 10p 50V 0201 RF_TR_2_B
BRF_ANT_M15_C C50067 10p 50V 0201 BRF_ANT_M15 [50]

Title: 50. Wi-Fi_BT
Microsoft Confidential
Engineer: Surface
Size A2
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
Sheet 50 of 79

5	4	3	2	1

D

C

B

A

Title: **51. Empty**

Microsoft Confidential

Engineer: ***Surface***

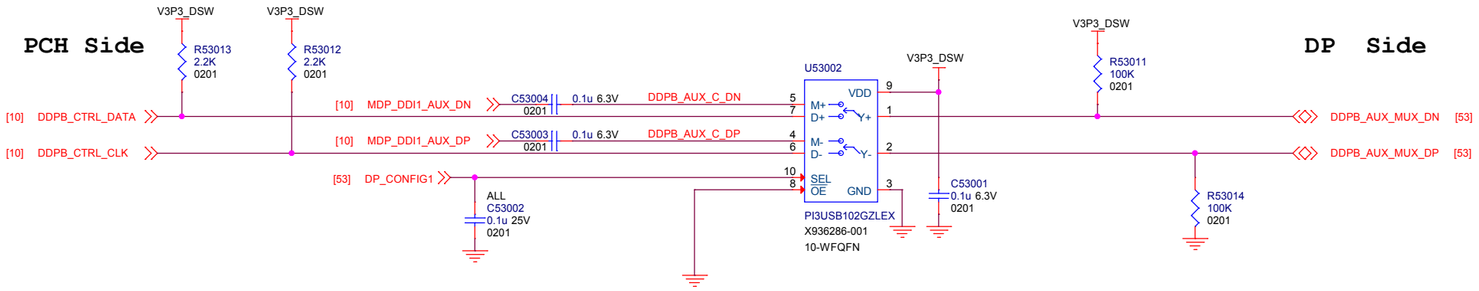
Size	Project Name	Rev
B	**A**	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 51 of 79

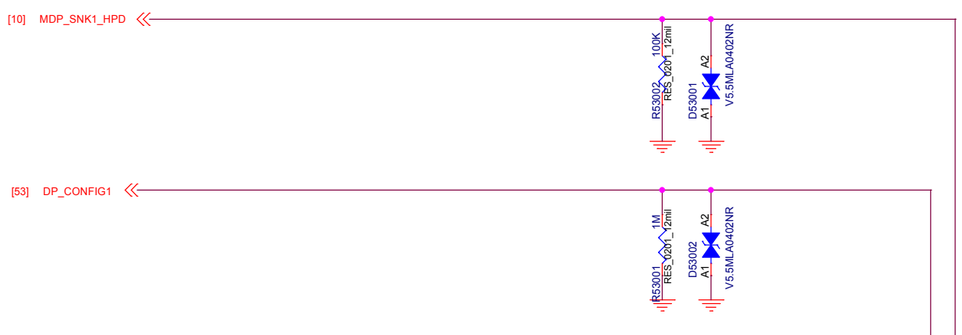
5 4 3 2 1

Title:	52. Empty		
Microsoft Confidential	Engineer:	*Surface*	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 52 of 79		

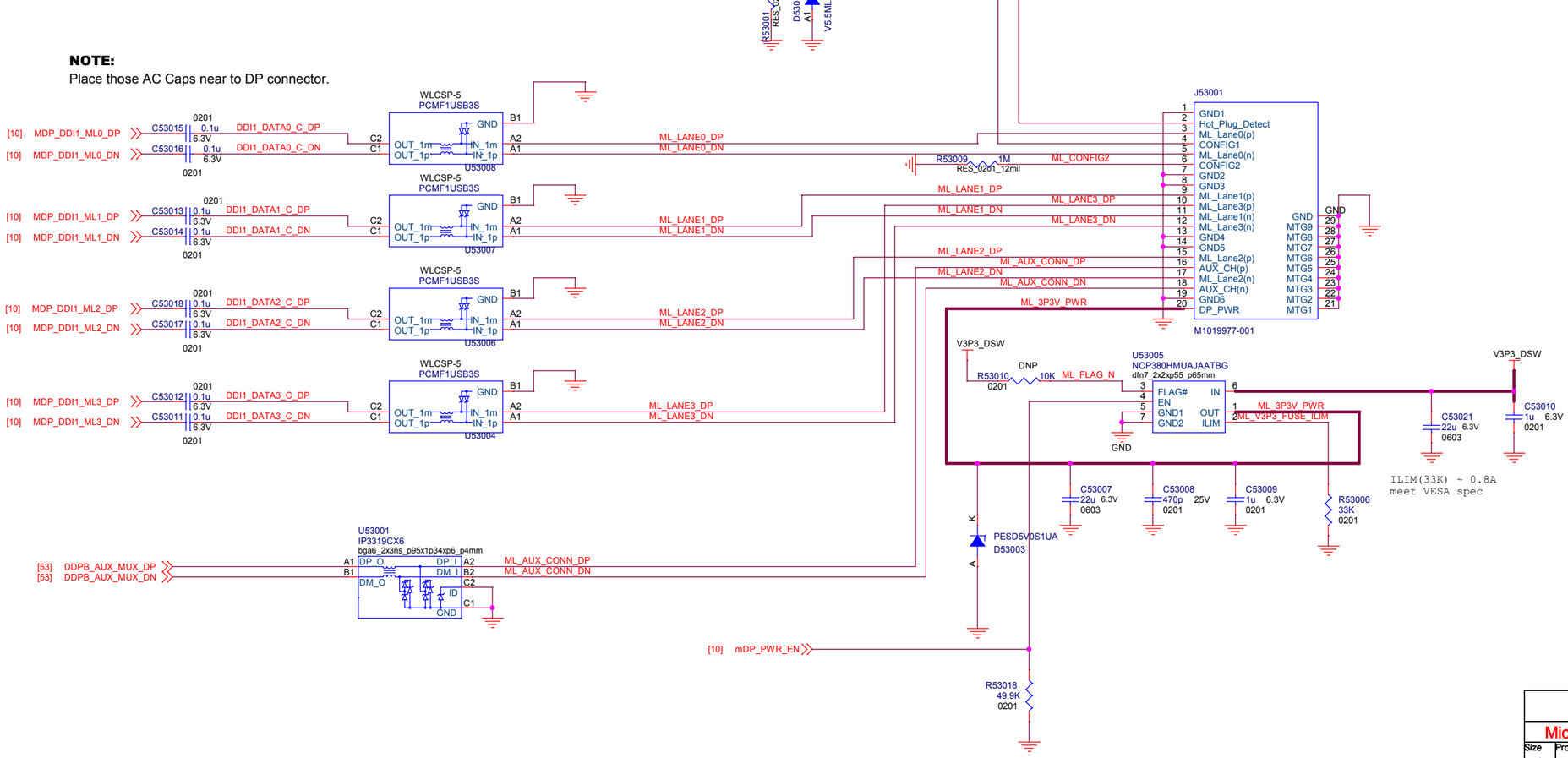
mDP mux to HDMI/DVI Dongle control



NOTE:
Place ESD Diodes close to DP connector



NOTE:
Place those AC Caps near to DP connector.



Title:	mDP		
Microsoft	Engineer:	Surface	
Size: C	Project Name: A		Rev: 2.89.6
Date: Thursday, April 26, 2018	Sheet 53 of 76		

Sensor Connector to IR and RGB Cameras, Left and Right Microphones, and ALS Sensor

To IR LED on FPC through J54001

RN54001, RN54002, RN54003, RN54005 need common footprint from DFX and to be stuffed with X869109-001

Layout Note: J54001 Pin 1 and Odd Pins along North Edge

Place caps close to U52001

Place close to pin 23

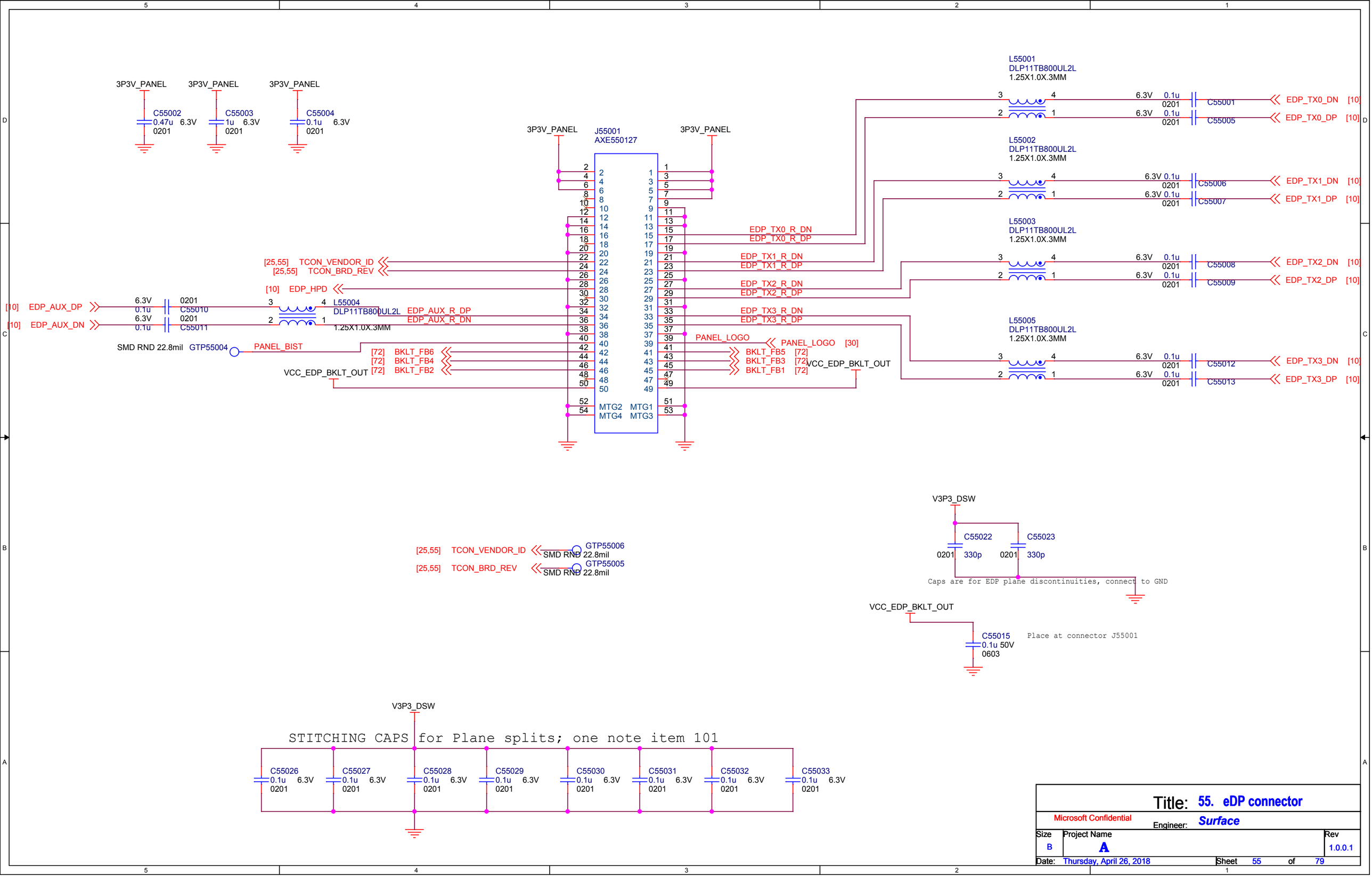
Place C54003 near connector

Pullups for I2C are on the Camera Flex.

ALS 7-bit I2C Address = 0x44
RGB Cam 7-bit I2C Address = 0x36
RGB EEPROM 7-bit I2C Address = TBD
IR Cam 7-bit I2C Address = 0x60

Check with Camera/RF/Power team for regulation, filtering, and component info
Power regulation, Privacy LED and sensors moved locally on sensor board. IRLED Buck regulation local to mb
Odd side of the J54001 connector faces the North edge of the PCB

Title:	54. Camera/Sensor Conn		
Microsoft Confidential	Engineer:	Surface	
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 54 of 79		



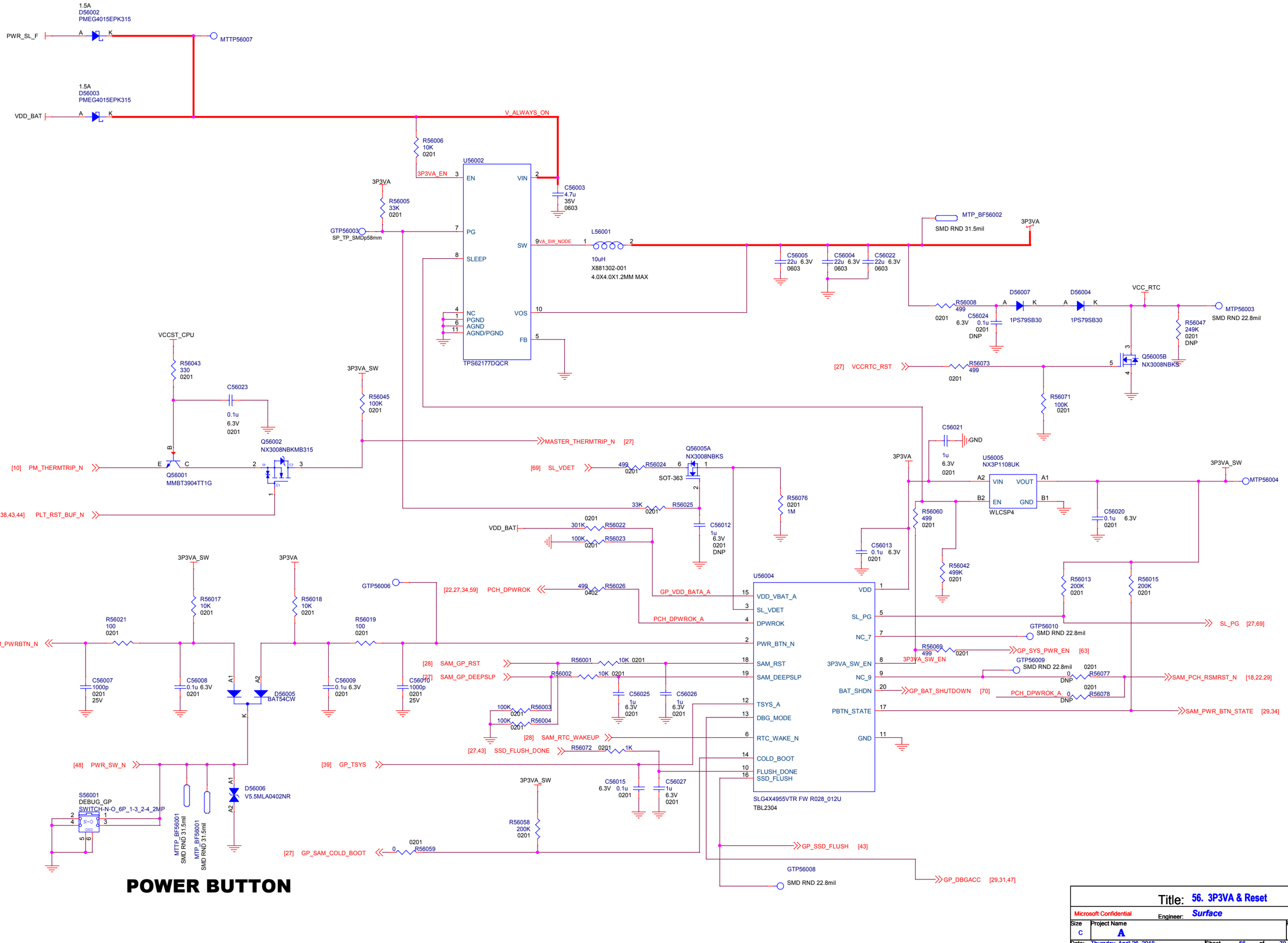
Title: 55. eDP connector

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 55 of 79


1.5A
D56002
PMEG4015EPK315
PWR_SL_F
MTTP56007
1.5A
D56003
PMEG4015EPK315
VDD_BAT
V_ALWAYS_ON
R56006
10K
0201
3P3VA_EN
U56002
EN
VIN
C56003
4.7u
35V
0603
3P3VA
R56005
33K
0201
GTP56003
SP_TP_SMDp58mm
PG
SW
9VA_SW_NODE
L56001
10uH
X881302-001
4.0X4.0X1.2MM MAX
SLEEP
NC
PGND
AGND
AGND/PGND
VOS
FB
TPS62177DQCR
C56005
22u 6.3V
0603
C56004
22u 6.3V
0603
C56022
22u 6.3V
0603
MTP_BF56002
SMD RND 31.5mil
3P3VA
R56008
499
0201
D56007
D56004
1PS79SB30
1PS79SB30
C56024
6.3V 0.1u
0201
DNP
VCC_RTC
MTP56003
SMD RND 22.8mil
R56047
249K
0201
DNP
[27] VCCRTC_RST
R56073
499
0201
Q56005B
NX3008NBKS
R56071
100K
0201
VCCST_CPU
R56043
330
0201
C56023
0.1u
6.3V
0201
Q56002
NX3008NBKMB315
3P3VA_SW
R56045
100K
0201
MASTER_THERMTRIP_N [27]
[10] PM_THERMTRIP_N
Q56001
MMBT3904TT1G
[22,27,34,38,43,44] PLT_RST_BUF_N
[69] SL_VDET
R56024
499
0201
Q56005A
NX3008NBKS
SOT-363
R56076
0201
1M
33K
R56025
0201
C56012
1u
6.3V
0201
DNP
VDD_BAT
301K
R56022
100K
R56023
0201
C56021
1u
6.3V
0201
GND
3P3VA
U56005
NX3P1108UK
VIN
VOUT
EN
GND
WLCSP4
3P3VA_SW
MTP56004
R56060
499
0201
C56020
0.1u 6.3V
0201
C56013
0.1u 6.3V
0201
R56042
499K
0201
R56013
200K
0201
R56015
200K
0201
U56004
3P3VA_SW
3P3VA
R56017
10K
0201
R56018
10K
0201
GTP56006
[22,27,34,59] PCH_DPWROK
R56026
499
0402
GP_VDD_BATA_A
PCH_DPWROK_A
R56021
100
0201
R56019
100
0201
[29] SAM_PWRBTN_N
C56007
1000p
0201
25V
C56008
0.1u 6.3V
0201
C56009
0.1u 6.3V
0201
C56010
1000p
0201
25V
D56005
BAT54CW
[28] SAM_GP_RST
[27] SAM_GP_DEEPSLP
R56001
10K 0201
R56002
10K 0201
C56025
1u
6.3V
0201
C56026
1u
6.3V
0201
100K
R56003
100K
R56004
[28] SAM_RTC_WAKEUP
[27,43] SSD_FLUSH_DONE
R56072 0201 1K
[48] PWR_SW_N
[39] GP_TSYS
D56006
V5.5MLA0402NR
S56001
DEBUG_GP
SWITCH-N-O_6P_1-3_2-4_2MP
MTTP_BF56001
SMD RND 31.5mil
MTP_BF56001
SMD RND 31.5mil
3P3VA_SW
R56058
200K
0201
C56015
6.3V 0.1u
0201
C56027
1u
6.3V
0201
[27] GP_SAM_COLD_BOOT
0
R56059
0201
SLG4X4955VTR FW R028_012U
TBL2304
GP_SSD_FLUSH [43]
GTP56008
SMD RND 22.8mil
GP_DBGACC [29,31,47]
VDD
SL_PG
NC_7
3P3VA_SW_EN
NC_9
BAT_SHDN
PBTN_STATE
GND
VDD_VBAT_A
SL_VDET
DPWROK
PWR_BTN_N
SAM_RST
SAM_DEEPSLP
TSYS_A
DBG_MODE
RTC_WAKE_N
COLD_BOOT
FLUSH_DONE
SSD_FLUSH
SL_PG [27,69]
GTP56010
SMD RND 22.8mil
R56069
499
0201
GP_SYS_PWR_EN [63]
3P3VA_SW_EN
GTP56009
SMD RND 22.8mil
R56077
0
DNP
SAM_PCH_RSMRST_N [18,22,29]
GP_BAT_SHUTDOWN [70]
PCH_DPWROK_A
R56078
0
DNP
SAM_PWR_BTN_STATE [29,34]
POWER BUTTON
Title: 56. 3P3VA & Reset
Microsoft Confidential
Engineer: Surface
Size C
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
Sheet 56 of 79

U SPECIFIC

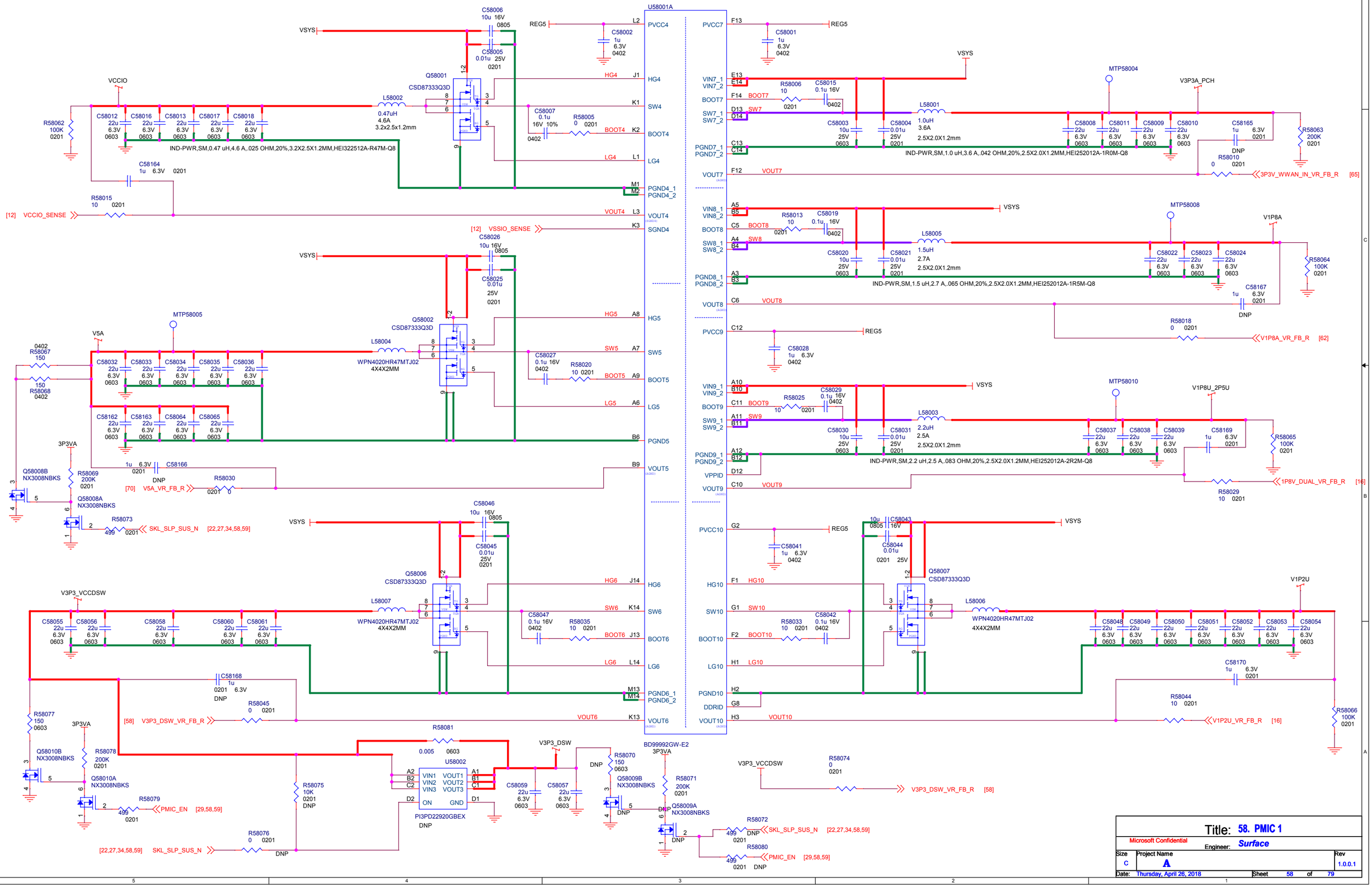
Title: 57. VCCEDRAM & VCCEOPIO

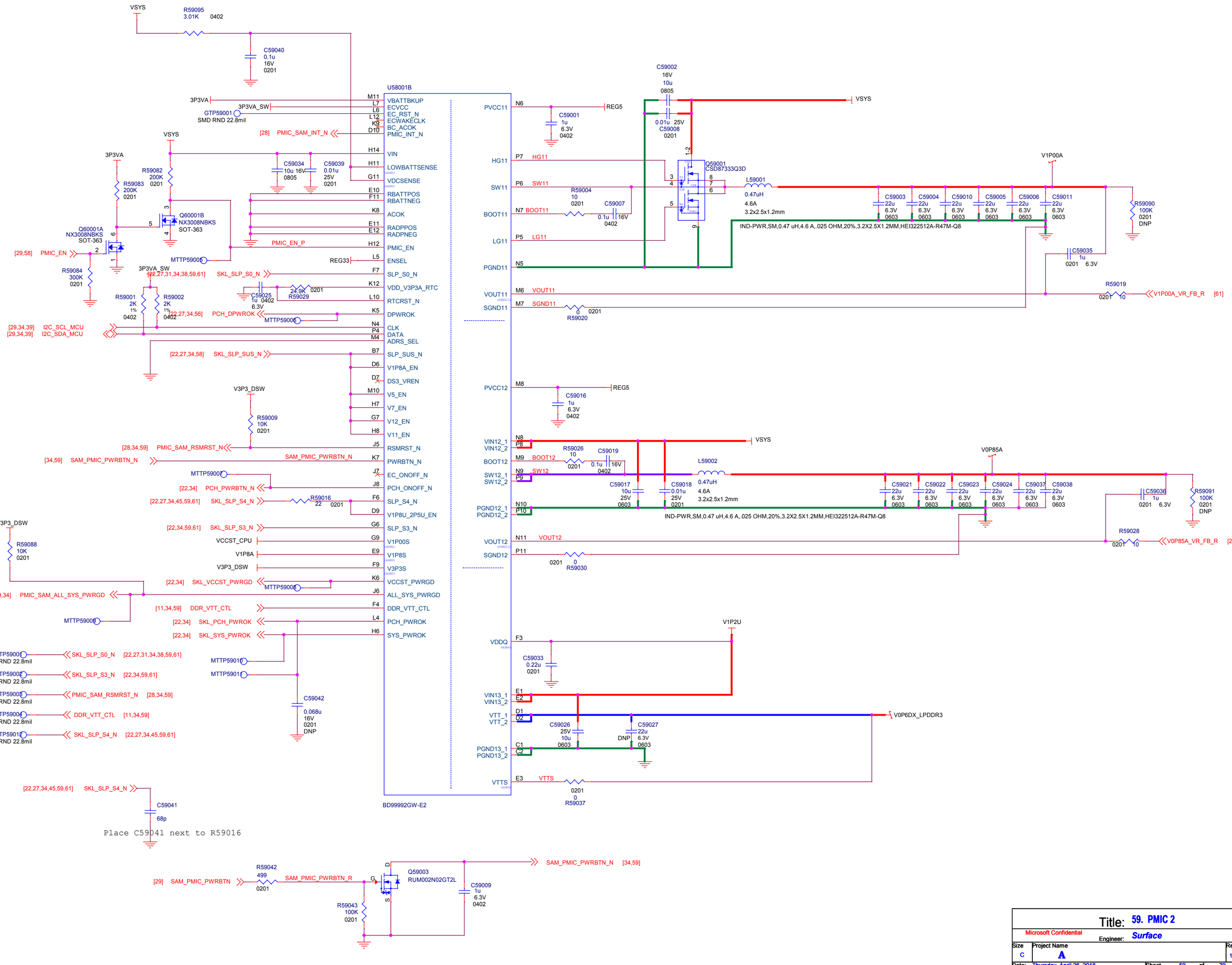
Microsoft Confidential

Engineer: *Surface*

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 57 of 79


U58001A
VSYS
VCCIO
REG5
C58006 10u 16V 0805
C58005 0.01u 25V 0201
C58002 1u 6.3V 0402
Q58001 CSD87333Q3D
L58002 0.47uH 4.6A 3.2x2.5x1.2mm
IND-PWR,SM,0.47 uH,4.6 A,.025 OHM,20%,3.2X2.5X1.2MM,HEI322512A-R47M-Q8
C58007 0.1u 16V 10%
R58005 0 0201
R58062 100K 0201
C58012 22u 6.3V 0603
C58016 22u 6.3V 0603
C58013 22u 6.3V 0603
C58017 22u 6.3V 0603
C58018 22u 6.3V 0603
C58164 1u 6.3V 0201
R58015 10 0201
[12] VCCIO_SENSE
[12] VSSIO_SENSE
HG4 J1 HG4
K1 SW4
BOOT4 K2 BOOT4
LG4 L1 LG4
M1 M2 PGND4_1 PGND4_2
VOUT4 L3 VOUT4
K3 SGND4
C58026 10u 16V 0805
C58025 0.01u 25V 0201
Q58002 CSD87333Q3D
L58004 WPN4020HR47MTJ02 4X4X2MM
C58027 0.1u 16V 0402
R58020 10 0201
HG5 A8 HG5
SW5 A7 SW5
BOOT5 A9 BOOT5
LG5 A6 LG5
B6 PGND5
B9 VOUT5
MTP58005
V5A
0402 R58067 150
150 R58068 0402
C58032 22u 6.3V 0603
C58033 22u 6.3V 0603
C58034 22u 6.3V 0603
C58035 22u 6.3V 0603
C58036 22u 6.3V 0603
C58162 22u 6.3V 0603
C58163 22u 6.3V 0603
C58064 22u 6.3V 0603
C58065 22u 6.3V 0603
3P3VA
Q58008B NX3008NBKS
Q58008A NX3008NBKS
R58069 200K 0201
R58073 499 0201
SKL_SLP_SUS_N [22,27,34,58,59]
C58166 1u 6.3V 0201 DNP
R58030 0201 0
[70] V5A_VR_FB_R
C58046 10u 16V 0805
C58045 0.01u 25V 0201
Q58006 CSD87333Q3D
L58007 WPN4020HR47MTJ02 4X4X2MM
C58047 0.1u 16V 0402
R58035 10 0201
HG6 J14 HG6
SW6 K14 SW6
BOOT6 J13 BOOT6
LG6 L14 LG6
M13 M14 PGND6_1 PGND6_2
VOUT6 K13 VOUT6
V3P3_VCCDSW
C58055 22u 6.3V 0603
C58056 22u 6.3V 0603
C58058 22u 6.3V 0603
C58060 22u 6.3V 0603
C58061 22u 6.3V 0603
C58168 1u 0201 6.3V DNP
R58045 0 0201
[58] V3P3_DSW_VR_FB_R
R58077 150 0603
Q58010B NX3008NBKS
Q58010A NX3008NBKS
R58078 200K 0201
R58079 499 0201
PMIC_EN [29,58,59]
R58076 0 0201 DNP
[22,27,34,58,59] SKL_SLP_SUS_N
R58081 0.005 0603
U58002
VIN1 VIN2 VIN3 VOUT1 VOUT2 VOUT3 ON GND A1 B1 C1 A2 B2 C2 D1 D2
PI3PD22920GBEX DNP
R58075 10K 0201 DNP
V3P3_DSW
C58059 22u 6.3V 0603
C58057 22u 6.3V 0603
BD99992GW-E2
3P3VA
R58070 150 0603 DNP
Q58009B NX3008NBKS
Q58009A NX3008NBKS
R58071 200K 0201 DNP
R58072 499 0201 DNP
SKL_SLP_SUS_N [22,27,34,58,59]
R58080 499 0201 DNP
PMIC_EN [29,58,59]
V3P3_VCCDSW
R58074 0 0201
V3P3_DSW_VR_FB_R [58]
PVCC7 F13 REG5
C58001 1u 6.3V 0402
VIN7_1 VIN7_2 E13 E14
BOOT7 F14 BOOT7
SW7_1 SW7_2 D13 SW7 D14
PGND7_1 PGND7_2 C13 C14
VOUT7 F12 VOUT7
R58006 10 0201
C58015 0.1u 16V 0402
C58003 10u 25V 0603
C58004 0.01u 25V 0201
L58001 1.0uH 3.6A 2.5X2.0X1.2mm
IND-PWR,SM,1.0 uH,3.6 A,.042 OHM,20%,2.5X2.0X1.2MM,HEI252012A-1R0M-Q8
MTP58004
V3P3A_PCH
C58008 22u 6.3V 0603
C58011 22u 6.3V 0603
C58009 22u 6.3V 0603
C58010 22u 6.3V 0603
C58165 1u 6.3V 0201 DNP
R58010 0 0201
R58063 200K 0201
3P3V_WWAN_IN_VR_FB_R [65]
VIN8_1 VIN8_2 A5 B5
BOOT8 C5 BOOT8
SW8_1 SW8_2 A4 SW8 B4
PGND8_1 PGND8_2 A3 B3
VOUT8 C6 VOUT8
R58013 10 0201
C58019 0.1u 16V 0402
C58020 10u 25V 0603
C58021 0.01u 25V 0201
L58005 1.5uH 2.7A 2.5X2.0X1.2mm
IND-PWR,SM,1.5 uH,2.7 A,.065 OHM,20%,2.5X2.0X1.2MM,HEI252012A-1R5M-Q8
MTP58008
V1P8A
C58022 22u 6.3V 0603
C58023 22u 6.3V 0603
C58024 22u 6.3V 0603
C58167 1u 6.3V 0201 DNP
R58064 100K 0201
R58018 0 0201
V1P8A_VR_FB_R [62]
PVCC9 C12 REG5
C58028 1u 6.3V 0402
VIN9_1 VIN9_2 A10 B10
BOOT9 C11 BOOT9
SW9_1 SW9_2 A11 SW9 B11
PGND9_1 PGND9_2 A12 B12
VPPID D12
VOUT9 C10 VOUT9
R58025 10 0201
C58029 0.1u 16V 0402
C58030 10u 25V 0603
C58031 0.01u 25V 0201
L58003 2.2uH 2.5A 2.5X2.0X1.2mm
IND-PWR,SM,2.2 uH,2.5 A,.083 OHM,20%,2.5X2.0X1.2MM,HEI252012A-2R2M-Q8
MTP58010
V1P8U_2P5U
C58037 22u 6.3V 0603
C58038 22u 6.3V 0603
C58039 22u 6.3V 0603
C58169 1u 6.3V 0201
R58065 100K 0201
R58029 10 0201
1P8V_DUAL_VR_FB_R [16]
PVCC10 G2 REG5
C58041 1u 6.3V 0402
HG10 F1 HG10
SW10 G1 SW10
BOOT10 F2 BOOT10
LG10 H1 LG10
PGND10 H2
DDRID G8
VOUT10 H3 VOUT10
C58043 10u 0805 16V
C58044 0.01u 0201 25V
Q58007 CSD87333Q3D
L58006 WPN4020HR47MTJ02 4X4X2MM
R58033 10 0201
C58042 0.1u 16V 0402
C58048 22u 6.3V 0603
C58049 22u 6.3V 0603
C58050 22u 6.3V 0603
C58051 22u 6.3V 0603
C58052 22u 6.3V 0603
C58053 22u 6.3V 0603
C58054 22u 6.3V 0603
V1P2U
C58170 1u 6.3V 0201
R58044 10 0201
R58066 100K 0201
V1P2U_VR_FB_R [16]
Title: 58. PMIC 1
Microsoft Confidential
Engineer: Surface
Size C
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
Sheet 58 of 79



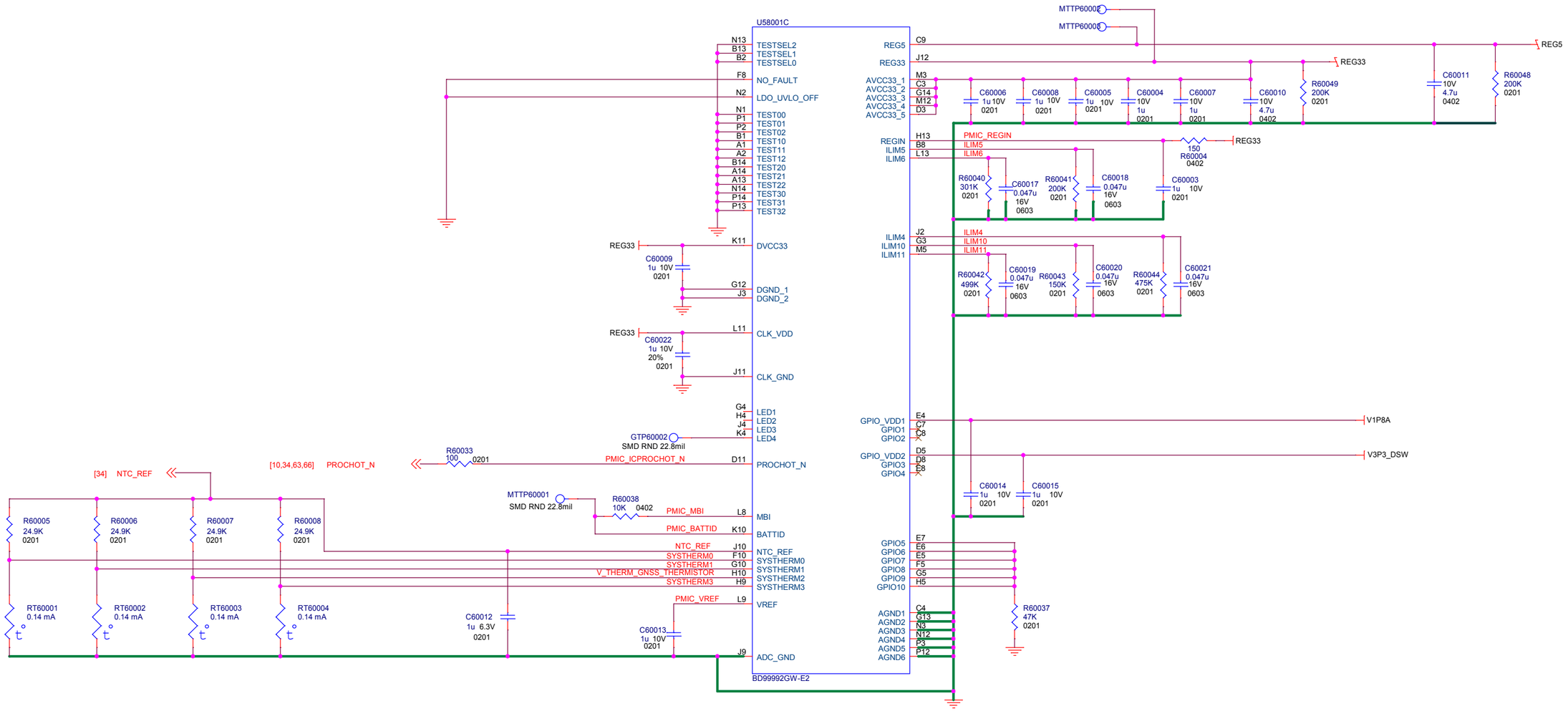
Microsoft Confidential

Title: 59. PMIC 2

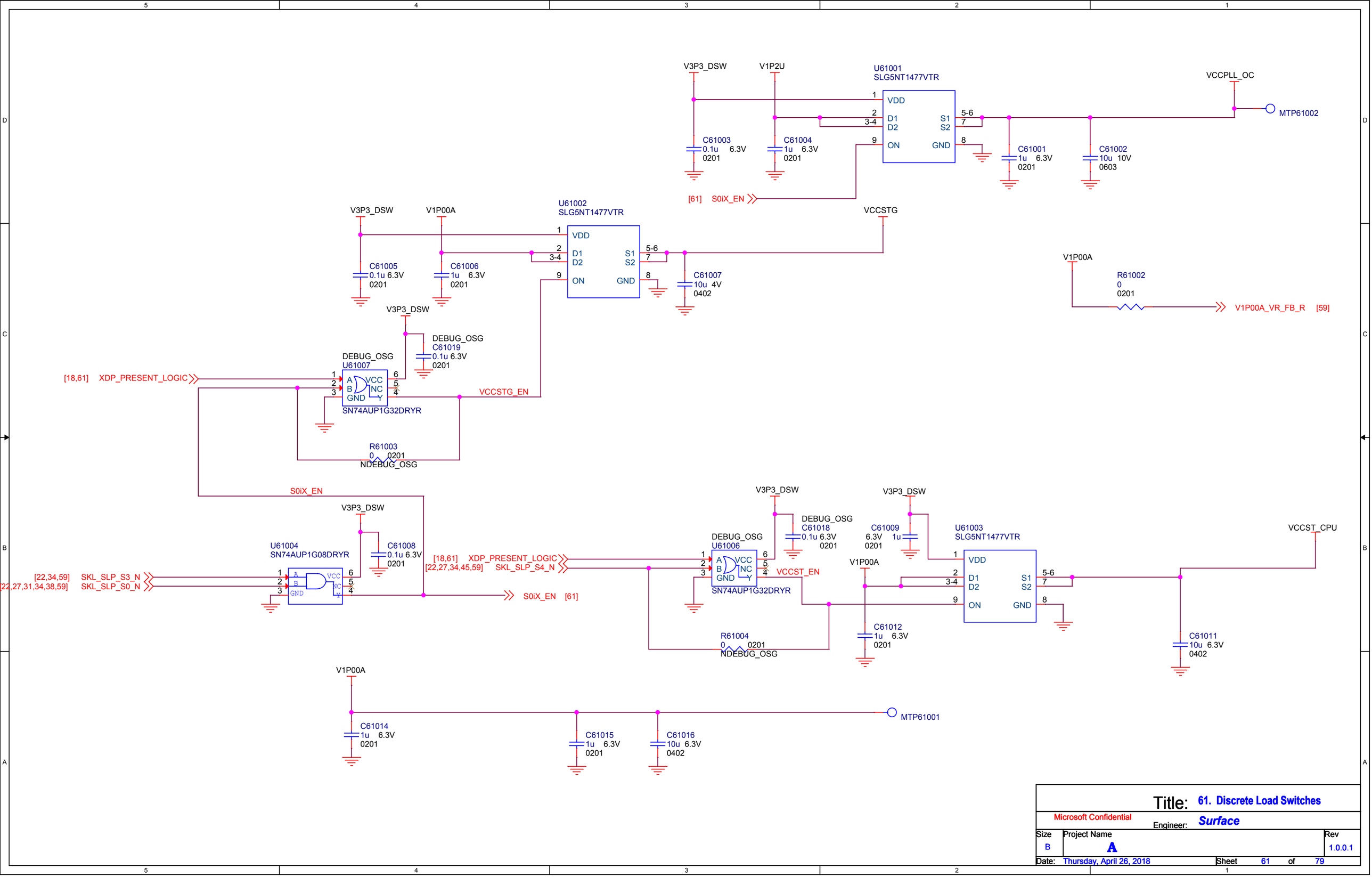
Engineer: Surface

Size	Project Name	Rev
C	A	1.0.0.1

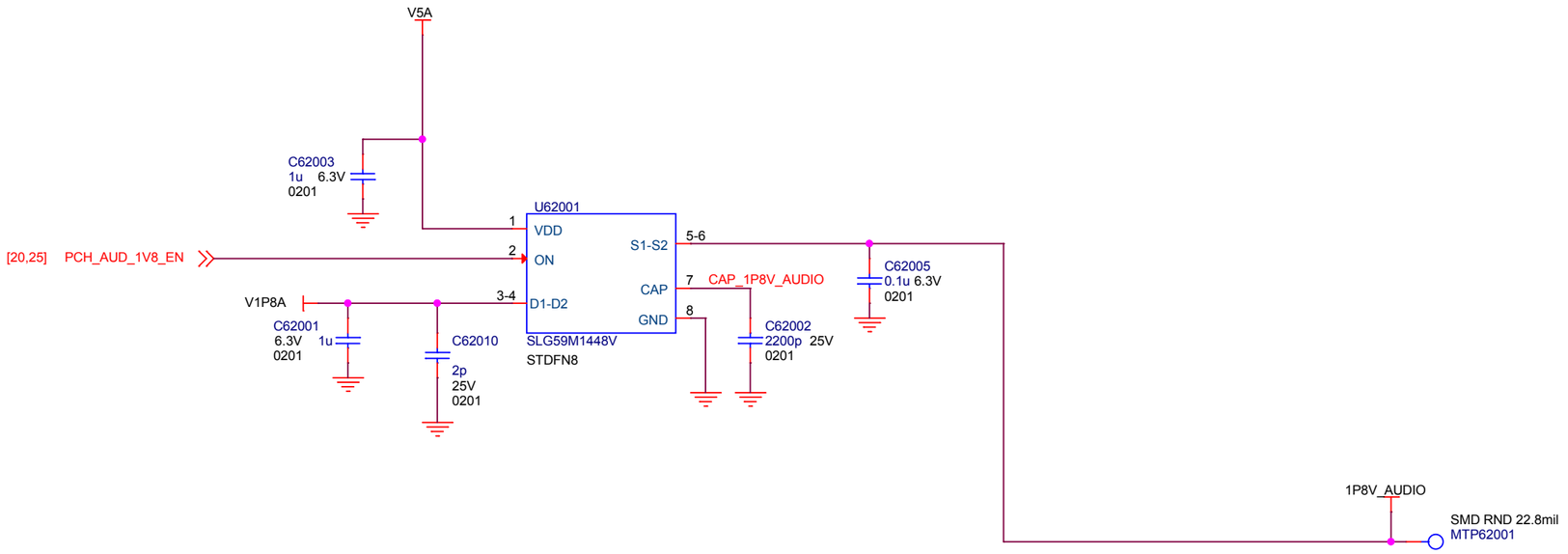
Date: Thursday, April 26, 2018 Sheet 59 of 79

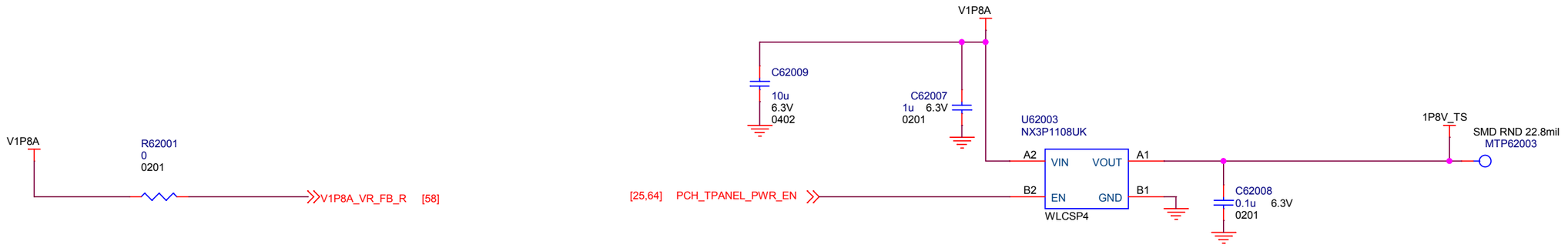


Title: 60. PMIC 3		
Microsoft Confidential	Engineer: Surface	
Size: C	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 60 of 79	

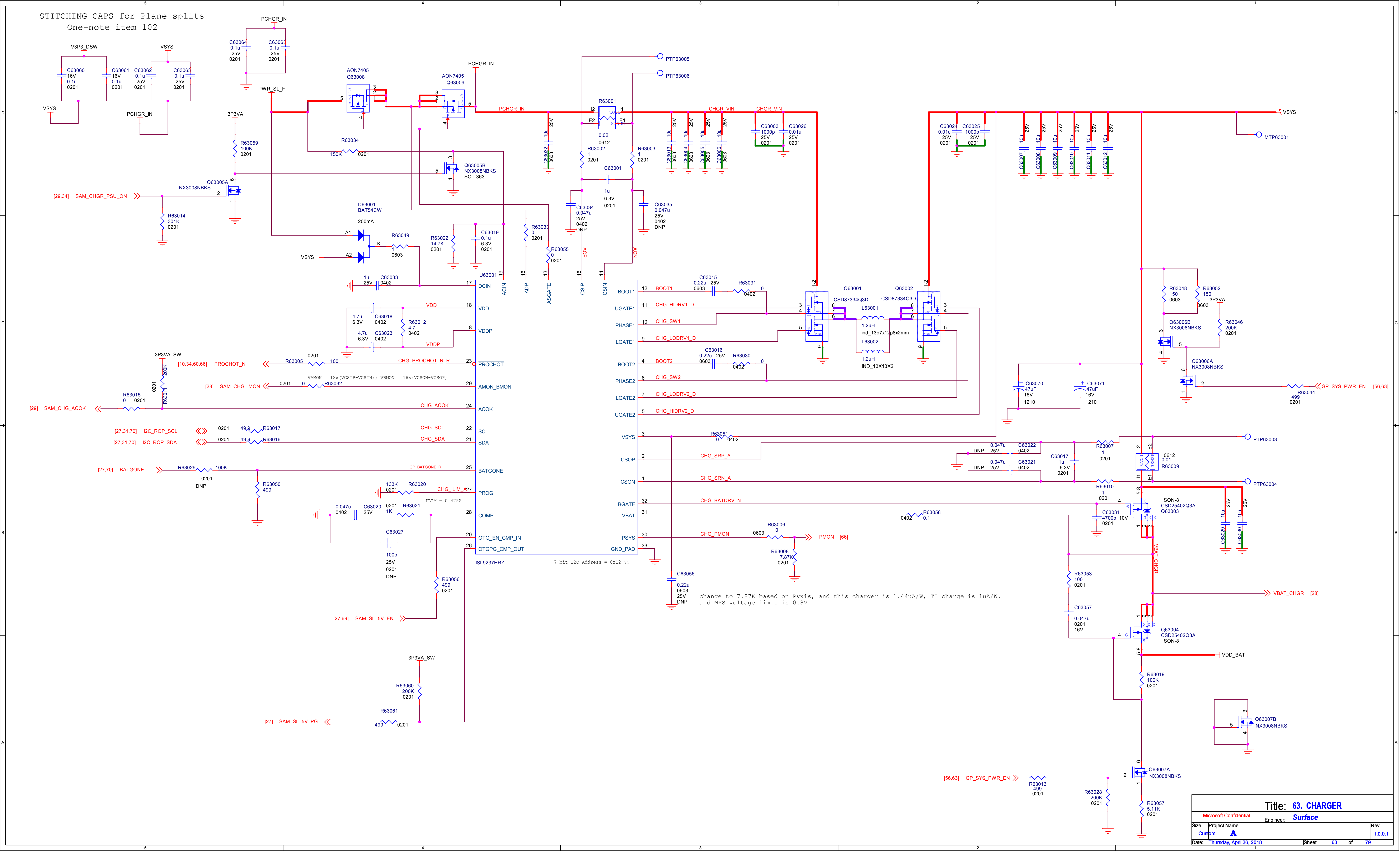


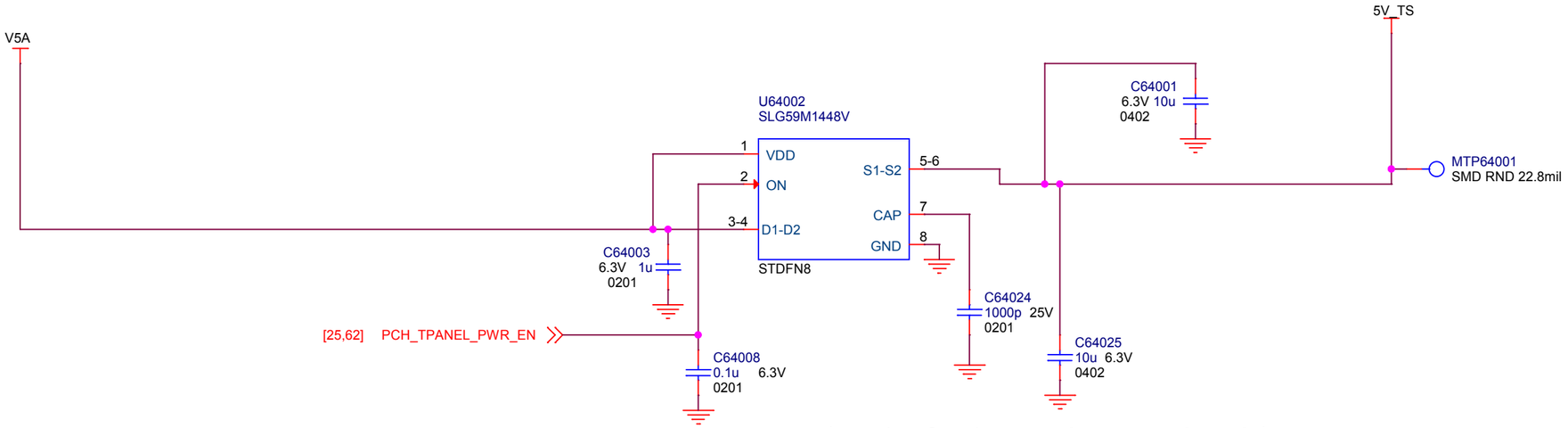
Title:	61. Discrete Load Switches	
Microsoft Confidential	Engineer: Surface	
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 61 of 79	



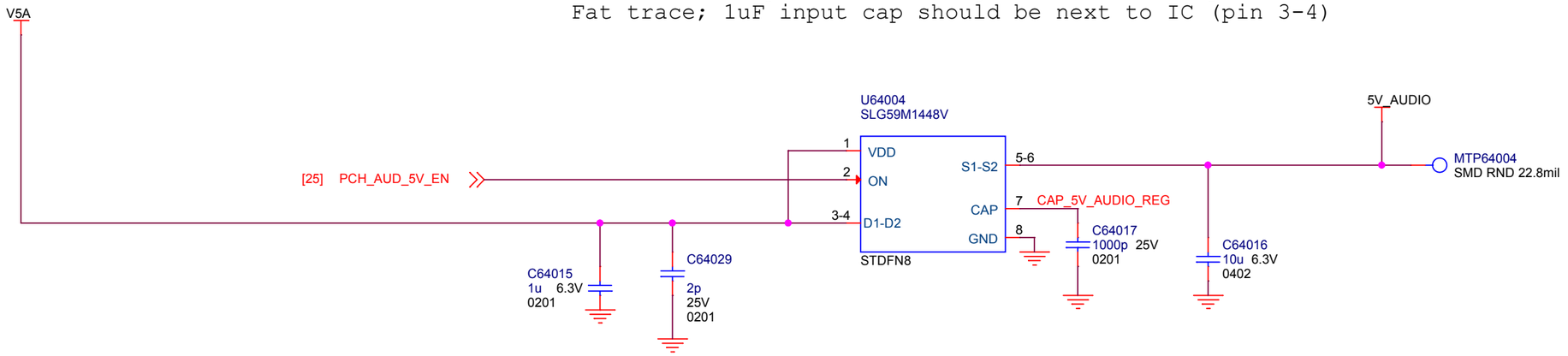


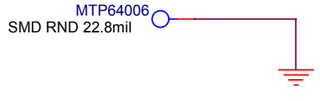
Title:	62. +1.8VSB & Load SW	
Microsoft Confidential	Engineer: Surface	
Size: A3	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 62 of 79	


STITCHING CAPS for Plane splits
One-note item 102
V3P3_DSW
VSYS
PCHGR_IN
PWR_SL_F
3P3VA
AON7405
Q63008
AON7405
Q63009
R63001
0.02
0612
PTP63005
PTP63006
PCHGR_IN
CHGR_VIN
VSYS
MTP63001
R63059
100K
0201
Q63005A
NX3008NBKS
[29,34] SAM_CHGR_PSU_ON
R63014
301K
0201
R63034
150K
Q63005B
NX3008NBKS
SOT-363
D63001
BAT54CW
200mA
R63049
R63022
14.7K
C63019
0.1u
6.3V
R63033
R63055
C63001
1u
6.3V
C63034
0.047u
25V
0402
DNP
C63035
0.047u
25V
0402
DNP
ACP
ACN
U63001
DCIN
VDD
VDDP
PROCHOT
AMON_BMON
ACOK
SCL
SDA
BATGONE
PROG
COMP
OTG_EN_CMP_IN
OTGPG_CMP_OUT
ISL9237HRZ
ACIN
ADP
ASGATE
CSIP
CSIN
BOOT1
UGATE1
PHASE1
LGATE1
BOOT2
PHASE2
LGATE2
UGATE2
VSYS
CSOP
CSON
BGATE
VBAT
PSYS
GND_PAD
7-bit I2C Address = 0x12 ??
3P3VA_SW
[10,34,60,66] PROCHOT_N
R63005
100
CHG_PROCHOT_N_R
VAMON = 18x(VCSIP-VCSIN); VBMON = 18x(VCSON-VCSOP)
[28] SAM_CHG_IMON
R63032
[29] SAM_CHG_ACOK
R63015
CHG_ACOK
[27,31,70] I2C_ROP_SCL
R63017
49.9
CHG_SCL
[27,31,70] I2C_ROP_SDA
R63016
49.9
CHG_SDA
[27,70] BATGONE
R63029
100K
DNP
GP_BATGONE_R
R63050
499
R63020
133K
CHG_ILIM_A
ILIM = 0.475A
C63020
0.047u
R63021
1K
C63027
100p
25V
0201
DNP
R63056
499
0201
[27,69] SAM_SL_5V_EN
R63060
200K
0201
R63061
499
0201
[27] SAM_SL_5V_PG
BOOT1
CHG_HDRV1_D
CHG_SW1
CHG_LODRV1_D
BOOT2
CHG_SW2
CHG_LODRV2_D
CHG_HDRV2_D
C63015
0.22u
25V
0603
R63031
C63016
0.22u
25V
R63030
Q63001
CSD87334Q3D
Q63002
CSD87334Q3D
L63001
1.2uH
ind_13p7x12p8x2mm
L63002
1.2uH
IND_13X13X2
C63003
1000p
25V
C63026
0.01u
25V
C63024
0.01u
25V
C63025
1000p
25V
C63070
47uF
16V
1210
C63071
47uF
16V
1210
R63048
150
0603
R63052
150
0603
Q63006B
NX3008NBKS
R63046
200K
Q63006A
NX3008NBKS
R63044
499
[56,63] GP_SYS_PWR_EN
R63051
0
0402
PTP63003
CHG_SRP_A
CHG_SRN_A
C63022
0.047u
25V
DNP
C63021
0.047u
25V
DNP
C63017
1u
6.3V
R63007
R63009
0.01
0612
R63010
PTP63004
CHG_BATDRV_N
R63058
0.1
0402
C63031
4700p
10V
SON-8
CSD25402Q3A
Q63003
CHG_PMON
R63006
0603
R63008
7.87K
PMON [66]
C63056
0.22u
0603
25V
DNP
change to 7.87K based on Pyxis, and this charger is 1.44uA/W, TI charge is 1uA/W.
and MPS voltage limit is 0.8V
R63053
100
C63057
0.047u
16V
VBAT_CHGR
VBAT_CHGR [28]
Q63004
CSD25402Q3A
SON-8
VDD_BAT
R63019
100K
Q63007B
NX3008NBKS
Q63007A
NX3008NBKS
[56,63] GP_SYS_PWR_EN
R63013
499
R63028
200K
R63057
5.11K
Title: 63. CHARGER
Microsoft Confidential
Engineer: Surface
Size Custom
Project Name A
Rev 1.0.0.1
Date: Thursday, April 26, 2018
Sheet 63 of 79



Note: connect pins 1, 3, 4 together at the chip
Fat trace; 1uF input cap should be next to IC (pin 3-4)





U SPECIFIC

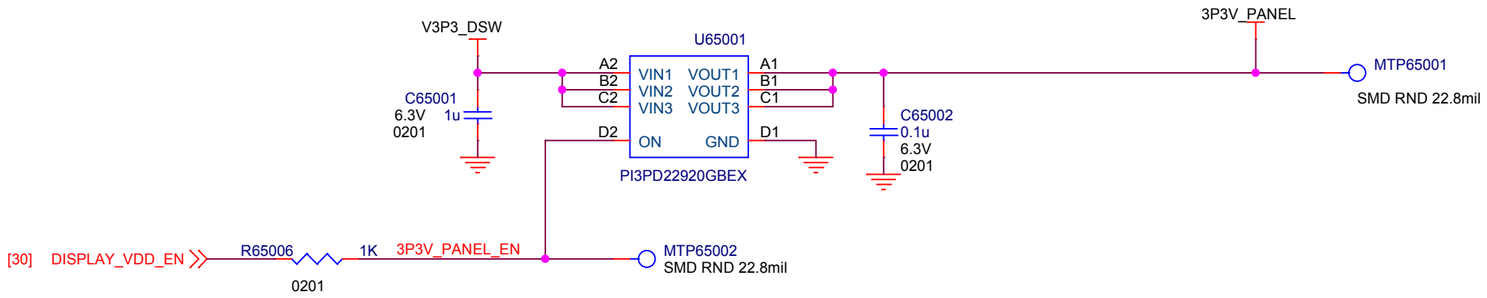
Microsoft Confidential

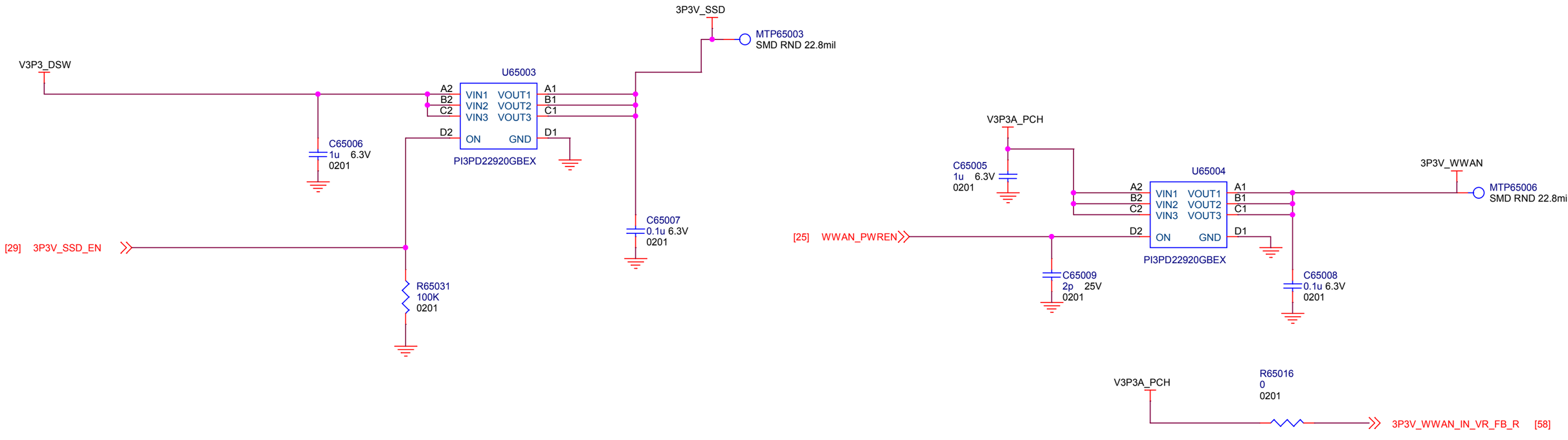
Title: 64. +5V Load SW

Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 64 of 79





Title: 65. +3P3V Load SW		
Microsoft Confidential	Engineer: Surface	
Size: B	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 65 of 79	

Scale to 0.80V for Psys Max.

Check Psys Settings

Should these be pull up to 3V3? VCCST?

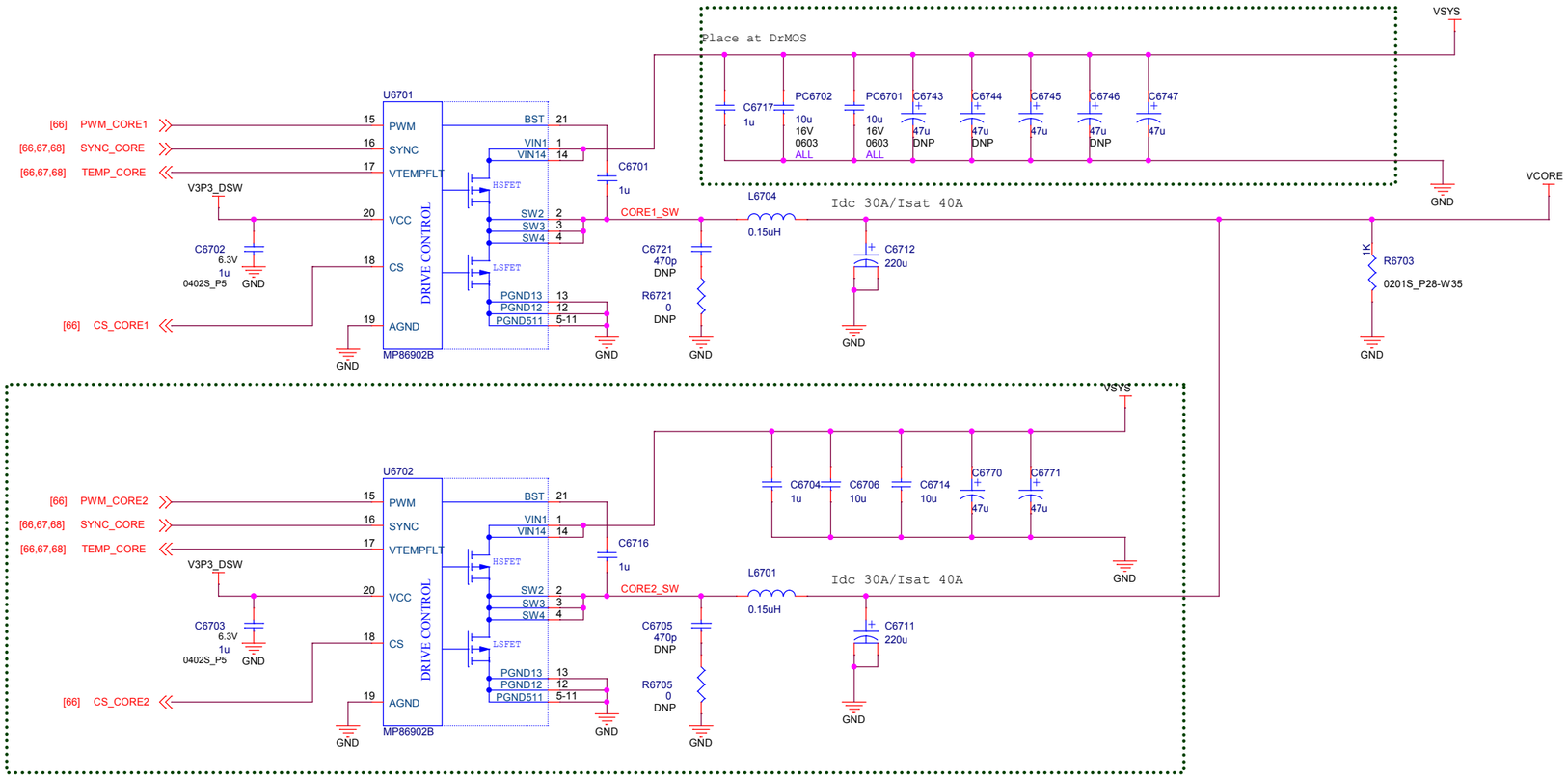
EV2.5 18 Oct 2016

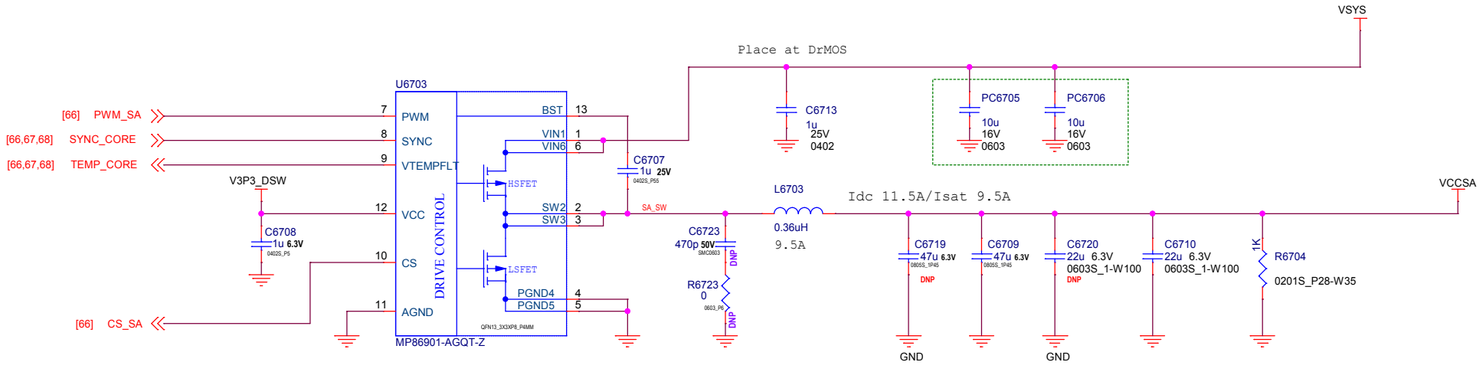
IMVP8 PROG

U SPECIFIC

Title:	66. VCPU Controller
Microsoft Confidential	Engineer: Surface
Size: C	Project Name: A
Rev:	1.0.0.1
Date:	Tuesday, May 01, 2018
Sheet	66 of 79

9V to 12V





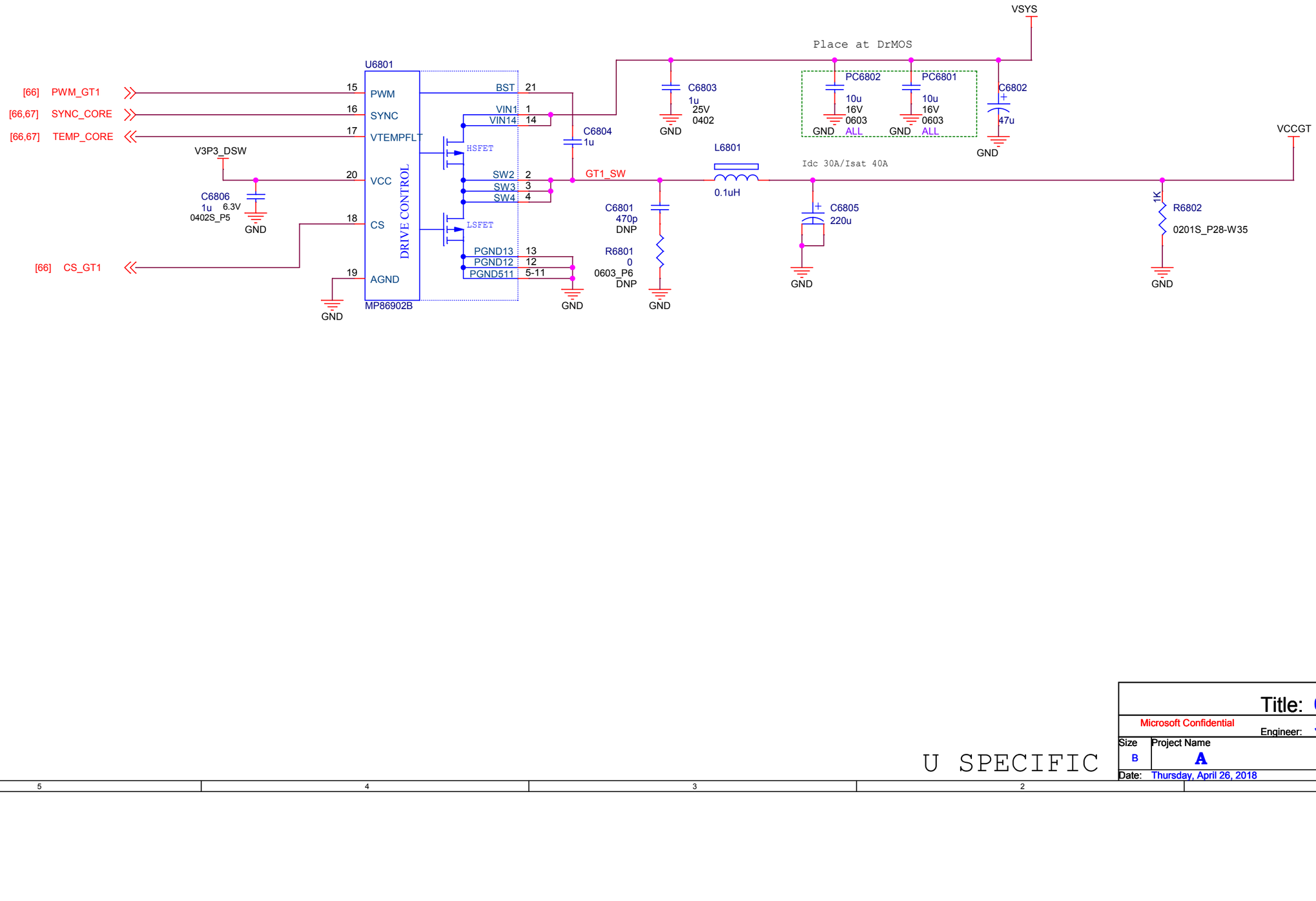
Title: 67. VCORE VCCSA

Microsoft Confidential

Engineer: Surface

Size	Project Name	Rev
C	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 67 of 79



U SPECIFIC

Microsoft Confidential

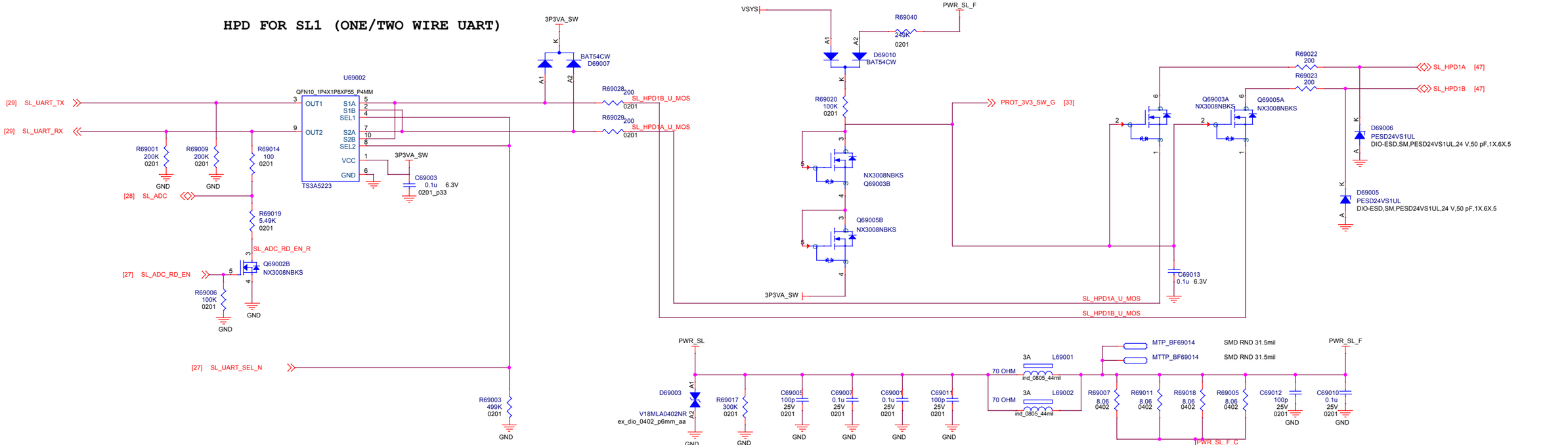
Title: 68. VCCGT

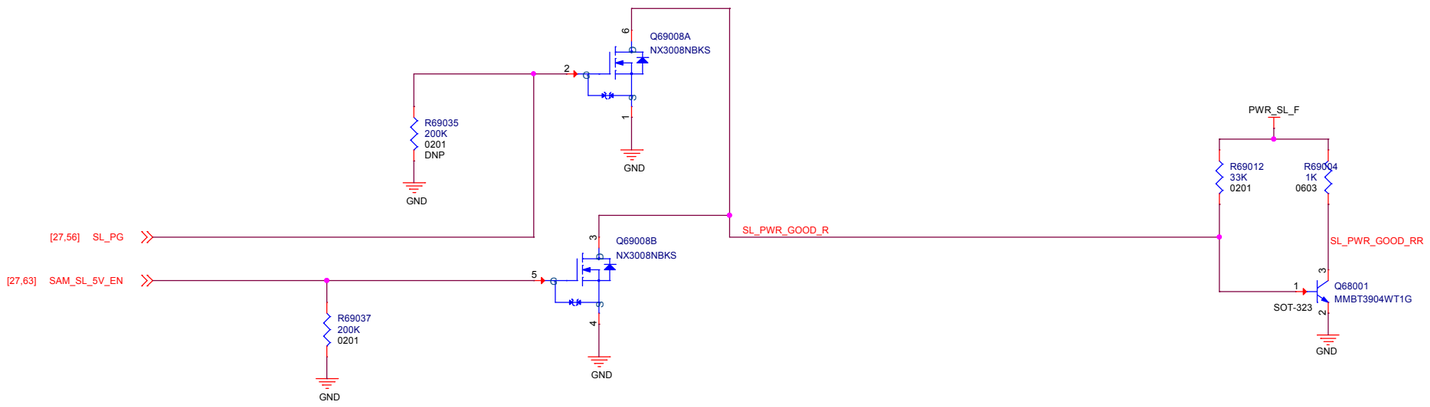
Engineer: Surface

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 68 of 79

HPD FOR SL1 (ONE/TWO WIRE UART)





SL1 port discharger
limit PSU anti-arc pulse voltage

Title: 69. SF1 POWER			
Microsoft Confidential	Engineer: Surface		
Size: A2	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 69 of 79		

Battery Connector

MTTP_BF70015 SMD RND 31.5mil
MTP_BF70015 SMD RND 31.5mil

V5A
R70040 0 0201
V5A_VR_FB_R [58]

VDD_BAT

R70042 100K 0201

J70003 2287111-2

J70003 to be place North of J70001
North of Board Edge

BAT_SHUTDOWN_N
[70] BATT_I2C_DATA

J70001 X950860-001

[70] BATT_I2C_CLK

J70002 2287111-2

Board Edge

[56] GP_BAT_SHUTDOWN
R70043 100 0201
R70041 100K 0201
Q70007 RUM002N02GT2L
3P3VA_SW
R70070 200K 0201
MTP70008 SMD RND 22.8mil
[27,63] BATGONE
MTP70007 SMD RND 22.8mil
MTP70005 SMD RND 22.8mil
MTP70006 SMD RND 22.8mil
TP70005 SMD SQ 29.5mil ***WHEN SHORTED BATTERY TURNS OFF***

NOTE: 1.7A/pin

Place TP's 0.2 inch apart,
Place on component side, near battery.
Must be accessible when battery is installed

C70015 0.1u 10V 0201

MTP_BF70001 SMD RND 31.5mil
MTP_BF70002 SMD RND 31.5mil
MTP_BF70003 SMD RND 31.5mil
MTP_BF70004 SMD RND 31.5mil
MTP_BF70005 SMD RND 31.5mil
MTP_BF70006 SMD RND 31.5mil
MTTP_BF70001 SMD RND 31.5mil
MTTP_BF70002 SMD RND 31.5mil
MTTP_BF70003 SMD RND 31.5mil
MTTP_BF70004 SMD RND 31.5mil
MTTP_BF70005 SMD RND 31.5mil
MTTP_BF70006 SMD RND 31.5mil

MTP_BF70007 SMD RND 31.5mil
MTP_BF70008 SMD RND 31.5mil
MTP_BF70009 SMD RND 31.5mil
MTP_BF70010 SMD RND 31.5mil
MTP_BF70011 SMD RND 31.5mil
MTP_BF70012 SMD RND 31.5mil
MTTP_BF70007 SMD RND 31.5mil
MTTP_BF70008 SMD RND 31.5mil
MTTP_BF70009 SMD RND 31.5mil
MTTP_BF70010 SMD RND 31.5mil
MTTP_BF70011 SMD RND 31.5mil
MTTP_BF70012 SMD RND 31.5mil

[27,31,63] I2C_ROP_SCL
L70001 0 0402
BATT_I2C_CLK [70]
MTP70003 SMD RND 22.8mil
DNP C70016 100p 16V 0201

[27,31,63] I2C_ROP_SDA
L70002 0 0402
BATT_I2C_DATA [70]
MTP70004 SMD RND 22.8mil
DNP C70017 100p 16V 0201

Title: 70. BATT CONN, power input
Microsoft Confidential
Engineer: Surface
Size A2 | Project Name A | Rev 1.0.0.1
Date: Thursday, April 26, 2018 | Sheet 70 of 79

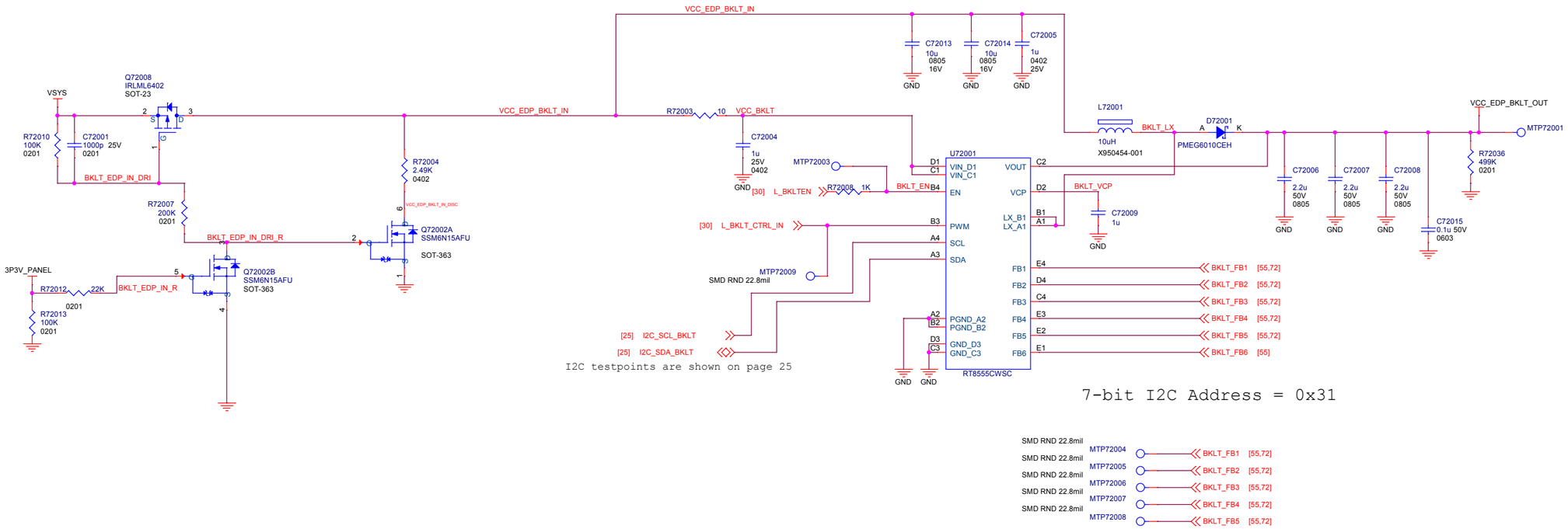
Title: 71. Empty

Microsoft Confidential

Engineer: *Surface*

Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 71 of 79



I2C testpoints are shown on page 25

7-bit I2C Address = 0x31

SMD RND 22.8mil MTP72004 BKLT_FB1 [55,72]
SMD RND 22.8mil MTP72005 BKLT_FB2 [55,72]
SMD RND 22.8mil MTP72006 BKLT_FB3 [55,72]
SMD RND 22.8mil MTP72007 BKLT_FB4 [55,72]
SMD RND 22.8mil MTP72008 BKLT_FB5 [55,72]

isolated ground on layer 2 to tie Cin GND, Cout GND, and controller PGND together. Then tie this isolated ground plane to main GND under the exposed pads.

Microsoft Confidential

Title: 72. Backlight Controller

Engineer: *Surface*

Size	Project Name	Rev
A2	A	1.0.0.1

Date: Tuesday, May 01, 2018 Sheet 72 of 79

Title:	73. Empty		
Microsoft Confidential	Engineer:		
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 73 of XX		

Title: 74. Empty

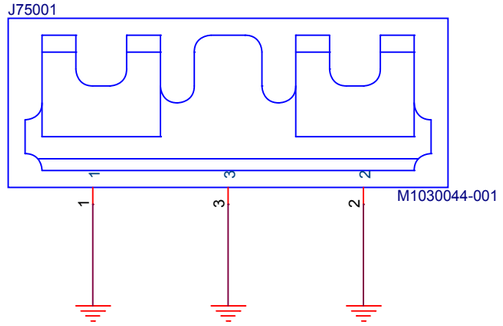
Microsoft Confidential

Engineer:

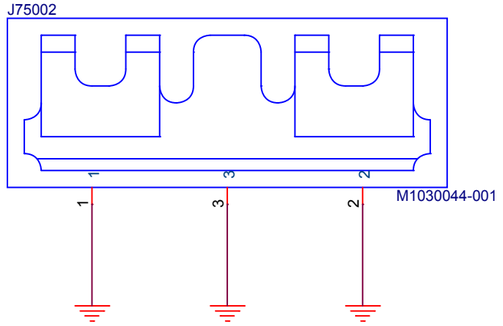
Size	Project Name	Rev
B	A	1.0.0.1

Date: Thursday, April 26, 2018 Sheet 74 of XX

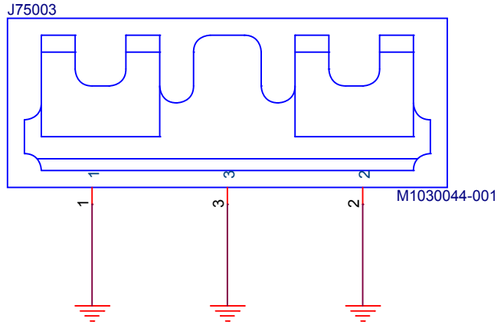
J75001



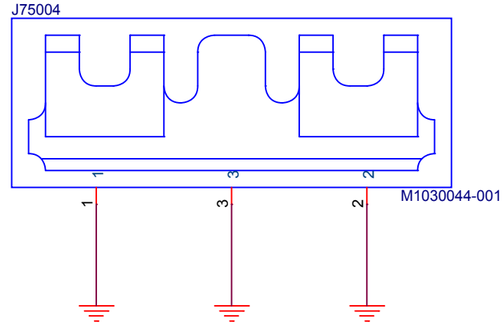
J75002



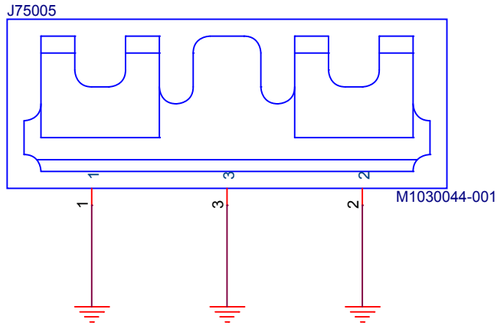
J75003



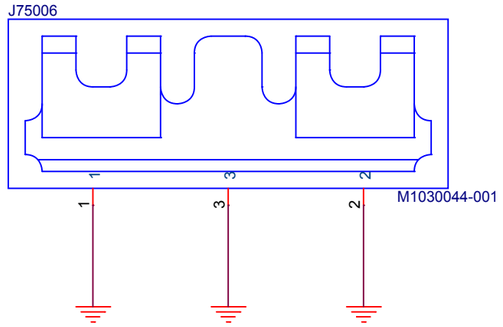
J75004



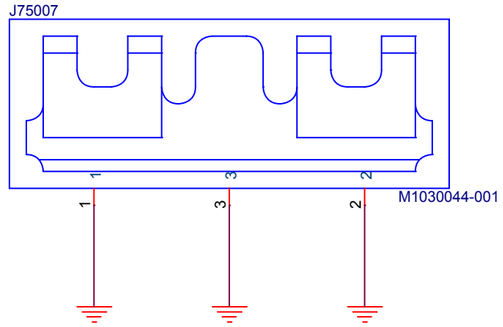
J75005



J75006



J75007



U SPECIFIC

Title: 75. Clips			
Microsoft Confidential	Engineer: Surface		
Size: B	Project Name: A		Rev: 1.0.0.1
Date: Thursday, April 26, 2018		Sheet 75 of 79	

BOTTOM SIDE spacers

MP76021 M1009352-002
MP76023 M1009352-002
MP76027 M1009352-002
MP76029 M1009352-002
MP76031 M1009352-002
MP76035 M1009352-002
MP76024 M1009352-002
MP76025 M1009352-002
MP76026 M1009352-002
MP76028 M1009352-002
MP76030 M1009352-002
MP76036 M1009352-002
MP76034 M1009352-002

VCCGT

TOP SIDE spacers

MP76033 M1012486-001
MP76032 M1012486-001
MP76037 M1012486-001
MP76038 M1012486-001

TOP SIDE spacers

MP76040 M1012486-001
MP76041 M1012486-001

MTP_BF76004 SMD RND 31.5mil
MTP_BF76005 SMD RND 31.5mil
MTP_BF76006 SMD RND 31.5mil
MTTP_BF76004 SMD RND 31.5mil
MTTP_BF76005 SMD RND 31.5mil
MTTP_BF76006 SMD RND 31.5mil

V0P85A — MTP76001 SMD RND 22.8mil
VCCGT — MTP76003 SMD RND 22.8mil
VCCSA — MTP76004 SMD RND 22.8mil
VCCIO — MTP76005 SMD RND 22.8mil
VCCST_CPU — MTP76006 SMD RND 22.8mil
VCCSTG — MTP76007 SMD RND 22.8mil

COAX Clips

MP76013 FCAU137A02C5PC X943446-001
MP76014 FCAU137A02C5PC X943446-001
MP76015 FCAU137A02C5PC X943446-001
MP76016 FCAU137A02C5PC X943446-001
MP76017 FCAU137A02C5PC X943446-001

PEMNUT for SoCs

MP76002 M1019199-001
MP76003 M1019199-001
MP76004 M1019199-001
MP76005 M1019199-001

PEMNUT for XDP

MP76042 M1019383-001

Shield Fences

SOC/SSD

SHT76001 M1016647-001 ZID = 00 ZOD = 00
SHT76002 X949514-001 ZID = 00 ZOD = 00 — PMIC
SHT76003 X949515-001 ZID = 00 ZOD = 00 — Charger
SHT76004 M1016649-001 ZID = 00 ZOD = 00 — Audio
SHT76005 X949517-001 ZID = 00 ZOD = 00 — Backlight/USB
SHT76006 M1016651-001 ZID = 00 ZOD = 00 — G5/Touch
SHT76007 M1016652-001 ZID = 00 ZOD = 00 — Display/Camera
SHT76008 X949521-001 ZID = 00 ZOD = 00 — Wi-Fi
SHT76009 M1013613-001 ZID = 00 ZOD = 00 — Trackpad
SHT76010 X949524-001 ZID = 00 ZOD = 00 — Surflink
SHB76003 M1016654-001 ZID = 00 ZOD = 00 — Touch

2.3mm NPTH

H76022 NO-MSPN-00212

2.5mm NPTH

H76010 H76011 H76012 H76013 H76014 NO-MSPN-159
H76016 H76017 H76018 H76019 H76020 NO-MSPN-159

H76002 NO-MSPN-157
H76001 NO-MSPN-157

V1P2U — MTP76010 SMD RND 22.8mil
V0P6DX_LPDDR3 — MTP76011 SMD RND 22.8mil
VCORE — MTP76012 SMD RND 22.8mil

U SPECIFIC

Title:	76. TP's and Mech	
Microsoft Confidential	Engineer: Surface	
Size: C	Project Name: A	Rev: 1.0.0.1
Date: Thursday, April 26, 2018	Sheet 76 of 79	